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Simple Current-Mode Squaring and Square-Rooting Circuits: Applications of MO-CCCCTA

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Abstract

This work provides new designs of simple current-mode squaring and square-rooting circuits using multiple-output current controlled current conveyor transconductance amplifier (MO-CCCCTA) as an active building block. Since the proposed circuits need no other external components, they are capable of high-frequency operation and well fitted for IC fabrication. Furthermore, they are insensitive to ambient temperature and their gains can be controlled easily by adjusting the bias currents of MO-CCCCTA. Additionally, the effects of MO-CCCCTA non-idealities on the designed circuits have also been investigated and discussed. Simulation results generated through PSPICE software using TSMC 0.18 μm CMOS process parameters have been presented to justify the theoretical analysis. The static power consumption, bandwidth, and maximum linearity error in dc transfer characteristic measurement for the square-rooting circuit are found to be 0.17 mW, 445.63 MHz and 1.12 %, while for the squaring circuit they are 0.326 mW, 61.15 MHz and 2.38 %, respectively. The application of the reported circuits as a 2-input vector summation circuit has also been included to strengthen the design ideas.

Keywords: MO-CCCCTA, Squarer, Square-rooter, Vector summation circuit

Introduction

Current-mode circuit designing is an appealing research field for decades due to many potential advantages over their voltage-mode counterpart like-wider dynamic range, simpler circuitry, extended signal bandwidth, improved linearity and lower power consumption [1,2]. Squaring and square-rooting circuits are very important building blocks extensively used for continuous-time signal processing in analog instrumentation, measurement and communication systems [3]. The root-mean-square value of an arbitrary waveform can also be found employing these circuits [4]. Recently, analog circuit designing using different active building blocks has received a lot of attention. Though several squaring and square-rooting circuits using various active building blocks have been reported earlier, they are not free from limitations. Specifically, in [3], 1 squarer and 2 square-rooters using a single current differencing buffer amplifier (CDBA) were introduced, but all of them work in voltage-mode. Moreover, 2 MOSFETs and 1 resistor are needed additionally for the squarer, and 2/4 external MOSFETs are needed for the first/second square-rooter, respectively. The single second-generation current conveyor (CCII) based squaring and square-rooting circuits reported in [5] employing 2 MOSFETs and 1 resistor, also work in voltage-mode. Despite that, an extra buffer circuit is used in the square-rooting circuit. Two square-rooters (one in voltage-mode and another in current-mode) were presented in [4]. The voltage-mode configuration employed 2 second-generation current-controlled current conveyors (CCCIIs), 1 current-controlled resistor and 2 grounded resistors, while the current-mode circuit required 2 CCCIIs and 1 current-controlled resistor. Using only CCCIIs, another current-mode squarer and square-rooter were proposed in [6], but 2 and 3 CCCIIs were needed for the square-rooter and the squarer circuit, respectively. The OP-AMP based square-rooting circuits informed in [7-10] have the disadvantages that they use excessive passive components and operate in voltage-mode. Also, the circuits of [7-9] employ multiple OP-AMPs. Again, the squaring and square-rooting circuits introduced in [11] employing an OP-AMP and 2/4 MOSFETs are of voltage-modes. Employing a single operational transresistance amplifier (OTRA) and 3 MOSFETs another squaring [12] and square-rooting [13] circuit was proposed, but they are also of voltage-modes. The squaring and square-rooting circuits reported in [14] using 1 differential difference current conveyor (DDCC) and 2 MOSFETs needed a relatively large power supply. Besides, the square-

rooter also required 1 voltage follower and a voltage-to-current converter. A square-rooter circuit employing 1 operation transconductance amplifier (OTA), 1 buffer and 1 MOSFET was presented in [15], but the circuit works in voltage-mode. The squaring and/or square-rooting circuits reported in [16-20] use 3 or more OTAs. Using 2 current differencing transconductance amplifiers (CDTAs) squaring and square-rooting circuits were presented in [21], but the circuits cannot provide current outputs. The single multiple-output current through transconductance amplifier (MO-CTTA) based square-rooter and squarer circuit introduced in [22] required a large power supply. The current mode square-rooting circuits proposed in [23,24] needed 2 active building blocks - namely MO-CFTA and CCCDTA, respectively. The squarer proposed in [25] required 4 current-controlled current differencing buffer amplifiers (CCCDBAs).

In 2008, a new current-mode active device namely the current-controlled current conveyor transconductance amplifier (CCCCTA) was introduced, which is basically a modified version of the current conveyor transconductance amplifier (CCTA) [26]. It resembles the CCTA in all perspectives with an additional feature that its parasitic resistance, R_x, at the X terminal can be adjusted through an input bias current. Intuitively, the CCCCTA is a multifunction active device, which provides the chance to exploit its transconductance gain (g_m) and its parasitic resistance (R_x) to make a resistorless design. The multiple current output ports of the CCCCTA can be achieved easily by attaching additional current mirrors at the requisite output ports. In earlier literature, the MO-CCCCTA is shown to give a lot of flexibility in designing various analog signal processing circuits, such as oscillator [26-28], capacitance multiplier [29], inductance simulator [26,30], universal biquad filter [26,31], etc. However, to the best knowledge of the authors, no squaring or square-rooting circuit employing MO-CCCCTA has been reported so far in any open literature. This motivates the authors highly to design new current-mode squaring and square-rooting structures based on MO-CCCCTA.

The major goal of this paper is to propose simple current-mode squaring and square-rooting circuits using MO-CCCCTA as an active device. Usually, a squarer is realized by simply feeding identical inputs in a multiplier. However, the scheme struggles with distortions arising mainly from nonlinearity of the multiplier [6]. A different aspect of this paper is to employ simple architectures comprising only MO-CCCCTA active block. Since no other external component has been used here, they are capable of high frequency operation and well suited for IC implementation. Moreover, they have immunity to temperature drift and their transfer gains can be controlled easily by adjusting the bias currents of MO-CCCCTA. The performances of the designed circuits are examined through PSPICE simulations which demonstrate close agreement with theoretical anticipations. Additionally, the application of the reported structures as a 2-input vector summation circuit is also included to demonstrate their efficiency.

Circuit description and methodology

Basic concept of MO-CCCCTA

Since the designed circuits are based on MO-CCCCTA, a concise description of MO-CCCCTA has been given in this section. Actually, MO-CCCCTA is a combined form of CCCII and OTA [27]. The schematic symbol and the equivalent circuit of the MO-CCCCTA have been displayed in **Figures 1a** and **1b**, respectively. A possible CMOS structure of MO-CCCCTA is given in **Figure 2** which is a marginally modified version of the structure suggested in [27,31].

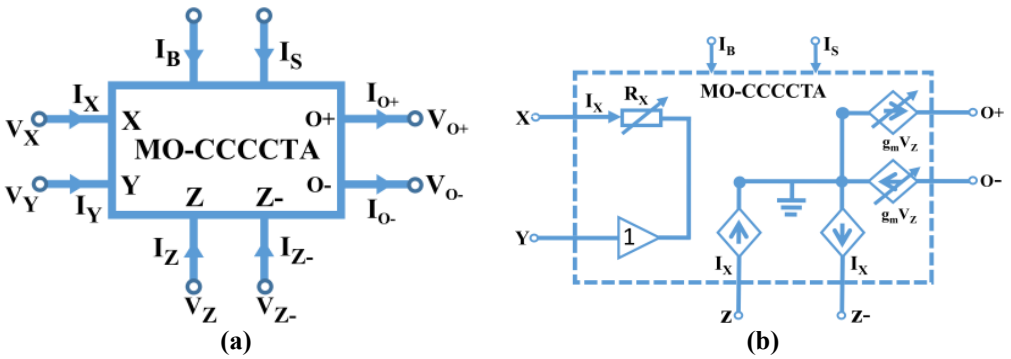

Figure 1 The MO-CCCCTA (a) schematic symbol and (b) equivalent circuit [28].

The ideal terminal characteristics of the MO-CCCCTA utilized in this article can be summarized by the following equation;

$$I_y = 0, V_x = V_y + I_x R_x, I_z = I_{zc} = -I_{z-} = I_x \text{ and } I_{O+} = -I_{O-} = g_m V_z \tag{1}$$

For a CMOS structure of MO-CCCCTA, the transconductance gain (g_m) and parasitic resistance (R_x) can be written as;

$$g_m = \sqrt{\mu_n C_{ox} \left(W/L\right)_{22,23} I_B} \text{ and } R_x = \frac{1}{\sqrt{8\mu_n C_{ox} \left(W/L\right)_{1,2} I_S}} \tag{2}$$

where μ_n and C_{ox} represent the mobility of electron and gate-oxide capacitance per unit area, respectively. $(W/L)_{1,2}$ represent the aspect ratio of M_1 or M_2 and $(W/L)_{22,23}$ represent the same for M_{22} or M_{23}. The bias currents I_B and I_S are used to control the transconductance gain and parasitic resistance, respectively.

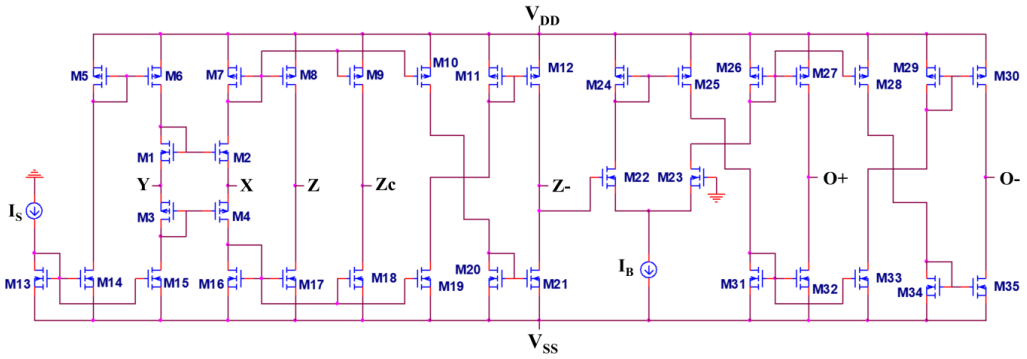

Figure 2 Internal structure of MO-CCCCTA utilizing CMOS transistors [27,31].

Basic concept of the designed circuit

The fundamental idea for devising the squaring and square-rooting circuits has been introduced at first in **Figure 3**. When both the switches S_1 and S_2 are opened and the MO-CCCCTA is with ideal characteristics, routine circuit analysis offers the following results;

$$I_{out} = I_{O-} = -g_m V_z \tag{3}$$

and

$$V_z = V_y = -I_{in} R_x \tag{4}$$

therefore,

$$I_{out} = g_m R_x I_{in} = \sqrt{\frac{\left(W/L\right)_{22,23} I_B}{8\left(W/L\right)_{1,2} I_S}} I_{in} \tag{5}$$

It is obvious from Eq. (5) that the circuit operates as a current amplifier. The magnitude of the output current (I_{out}) can be adjusted easily by controlling the bias current I_B and/or I_S. This basic idea has been used to realize the squaring and square-rooting circuits. The implementations of both the squaring and square-rooting circuits will be represented in the succeeding sections.

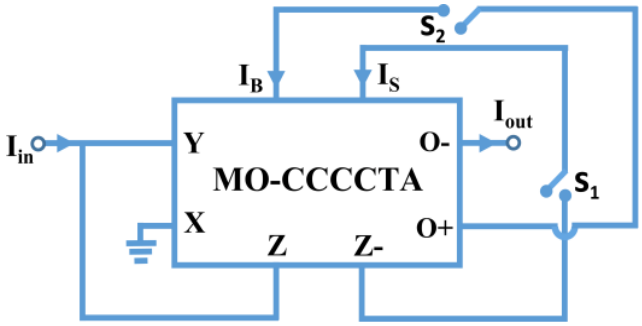

Figure 3 Basic diagram of the designed circuit.

Proposed square-rooting circuit

Eq. (5) clearly indicates that if I_{in} is put in for I_S, i.e., closing switch S_1 and opening switch S_2 in **Figure 3**, the output current (I_{out}) will be proportional to the square root of the input current (I_{in}). Its magnitude can be adjusted by tuning the bias current I_B. The expression for the output current of the proposed square-rooting circuit has been given in Eq. (6);

$$I_{out} = k\sqrt{I_B}\sqrt{I_{in}}; k = \left\{ \left(\frac{W}{L}\right)_{22,23} \Big/ 8\left(\frac{W}{L}\right)_{1,2} \right\}^{1/2} \tag{6}$$

Proposed squaring circuit

It is also evident from Eq. (5) that a squarer can be realized by putting I_{out} for I_B, i.e., opening switch S_1 and closing switch S_2 in the circuit of **Figure 3**. The squarer circuit provides the following output;

$$I_{out} = \frac{k^2}{I_S} I_{in}^{\ 2} \tag{7}$$

Clearly from Eq. (7), the output current (I_{out}) is directly proportional to the square of the input current (I_{in}). Its magnitude can be adjusted by controlling the bias current I_S. Note that the circuit operates only for the positive input. In order to get a squaring output for the bidirectional current input, another configuration has been put forward and displayed in **Figure 4**. A routine analysis shows that the circuit of **Figure 4** yields the output as follows;

$$I_{out} = I_{O1-} + I_{O2-} \tag{8}$$

where

$$I_{O1-} = \begin{cases} k^2 \dfrac{I_{in}^{\ 2}}{I_{S1}}, & I_{in} > 0 \\ 0, & I_{in} \le 0 \end{cases} \tag{9}$$

and

$$I_{O2-} = \begin{cases} k^2 \dfrac{I_{in}^{\ 2}}{I_{S2}}, & I_{in} < 0 \\ 0, & I_{in} \ge 0 \end{cases} \tag{10}$$

It is clear that the MO-CCCCTA-1 and the MO-CCCCTA-2 alternate for the positive and negative cycle of input current if $I_{S1} = I_{S2} = I_S$. The final output for the full input cycle is then obtained as;

$$I_{out} = k^2 \frac{I_{in}^{\ 2}}{I_S} \tag{11}$$

Evidently, the circuit of **Figure 4** is a true 4-quadrant squarer. However, it is gained at the expense of 1 extra MO-CCCCTA.

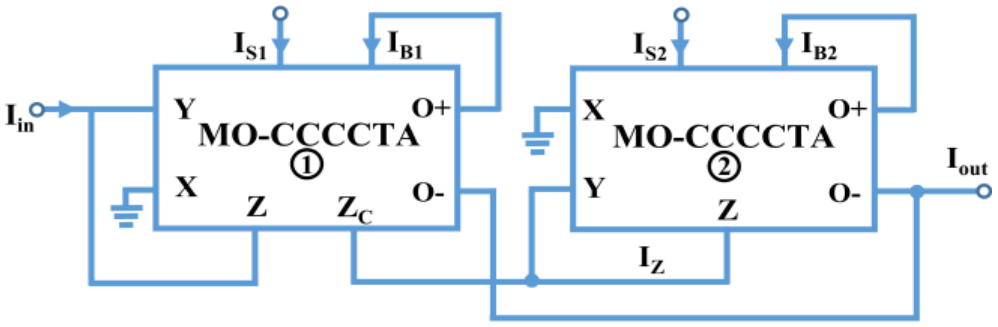

Figure 4 The completed current-mode squarer.

Non-ideality effects

The analysis in the preceding section is built on the ideal characteristics of the MO-CCCCTA. Practically, the reported circuits are deviated from their ideal performance due to the voltage/current gain errors and parasitic elements in MO-CCCCTA. Considering the voltage/current gain errors, the terminal relationships of MO-CCCCTA can be described as follows;

$$I_y = 0, V_x = \beta V_y + I_x R_x, I_z = \alpha_p I_x, I_{zc} = \alpha_{pc} I_x, I_{z-} = -\alpha_n I_x, I_{O+} = \gamma_p g_m V_z, \text{ and } I_{O-} = -\gamma_n g_m V_z \tag{12}$$

where α_p is the current transfer error from X terminal to Z terminal, α_{pc} is the current transfer error from X terminal to Z_C terminal, α_n is the current transfer error from X terminal to Z-terminal, β is the voltage transfer error from X terminal to Y terminal, γ_p is the current transfer error from X terminal to O+ terminal, and γ_n is the current transfer error from X terminal to O-terminal.

In addition, like any other active device, a practical MO-CCCCTA shows various terminals parasitic. **Figure 5** illustrates the well-established parasitic model of MO-CCCCTA [32]. A parasitic resistor R_X appears in series at X terminal, parasitic impedances in the form of $R_Y||C_Y$ appears at Y terminal, $R_Z||C_Z$ appears at Z terminal, $R_{Z-}||C_{Z-}$ appears at Z– terminal, $R_{O+}||C_{O+}$ appears at O+ terminal and $R_{O-}||C_{O-}$ appears at O– terminal. All the parasitic resistances are of high values, while the capacitances are of very low values. Taking the terminals parasitic of the MO-CCCCTAs into account and considering the gain errors stated in Eq. (12), the square-rooting circuit yields the following output;

$$I_{out} = \left(\frac{k\gamma_n}{\beta}\right)\sqrt{\frac{I_B}{\alpha_p \alpha_n}}\cdot\left[\frac{\sqrt{I_{in}}}{\sqrt{\left(1-b-\frac{s}{\omega'}\right)\left(1+c+\frac{s}{\omega''}\right)}}\right] \tag{13}$$

Similarly, the output current (I_{out}) of the basic squaring circuit is found as given in Eq. (14);

$$I_{out}=\frac{\gamma_p\gamma_n}{I_S}\left(\frac{k}{\beta\alpha_p}\right)^2\left[\frac{(I_{in})^2}{\left(1-b-\frac{s}{\omega'}\right)^2\left(1+c+\frac{s}{\omega''}\right)}\right] \tag{14}$$

Meanwhile, the squarer in **Figure 4** reflects the following output;

$$I_{outt}=\begin{cases}\dfrac{\gamma_{p1}\gamma_{n1}}{I_{S1}}\left(\dfrac{k}{\alpha_{p1}\beta_1}\right)^2\left[\dfrac{(I_{in})^2}{\left(1-b_1-\dfrac{s}{\omega_1'}\right)^2\left(1+c_1+\dfrac{s}{\omega_1''}\right)}\right] & \text{for } I_{in}>0\\ \dfrac{\gamma_{p2}\gamma_{n2}}{I_{S2}}\left(\dfrac{k\alpha_{pc1}}{\alpha_{p1}\alpha_{p2}\beta_2}\right)^2\left[\dfrac{(I_{in})^2}{\left[1-b_1-\dfrac{s}{\omega_1'}\right]^2\left(1+c_2+\dfrac{s}{\omega_2''}\right)\left[1-d-\dfrac{\left\{1+\frac{C_{Zc1}}{(C_{Y2}+C_{Z2})}\right\}}{\omega_2'}\right]^2}\right] & \text{for } I_{in}<0\end{cases} \tag{15}$$

where $b=\frac{R_X(R_Y+R_Z)}{\alpha_p\beta R_Y R_Z}$, $c=\frac{R_L}{R_{O-}}$, $d=\left(\frac{1}{R_{Y2}}+\frac{1}{R_{Z2}}+\frac{1}{R_{ZC1}}\right)\frac{R_{X1}}{\alpha_{p2}\beta_2}$, $\omega'=\frac{\alpha_p\beta}{R_X(C_Y+C_Z)}$, and $\omega''=\frac{1}{R_LC_{O-}}$; R_L is the load resistor and the suffix 1 represents the values of the parameters for block 1 (similarly for suffix 2). It is noted from Eqs. (13) - (15) that the non-idealities of the MO-CCCCTAs will cause minor changes in the transfer current gains. Moreover, the output currents may slightly depend on temperature, as the non-ideal tracking errors depend on temperature slightly. However, these deviations can be easily compensated by balancing the values of I_B and I_S for the square-rooting and squaring circuit, respectively. It is also noted that the useful frequency range (ω) of the proposed circuits are limited by the extra poles ω', ω'', ω_2' and ω_2'' which become effective at very high frequencies. Therefore, in order to minimize the influence of the MO-CCCCTAs' parasitics, the proper operation frequency should restrict to the following conditions [21];

$$\omega \le 0.1\omega'; 0.1\omega''; 0.1\omega_2'; \text{and } 0.1\omega_2'' \tag{16}$$

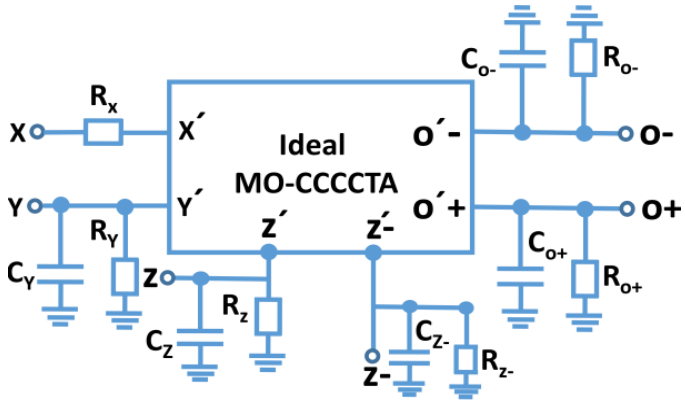

Figure 5 Parasitic model of MO-CCCCTA [32].

Simulation results

To confirm the theoretical predictions, the designed circuits were simulated by Cadence PSPICE program. In order to fulfill the MO-CCCCTA active device in simulations, it was realized by the schematic CMOS structure given in **Figure 2** with the TSMC 0.18 μm CMOS model parameters. All of the reported circuits are powered by ±0.9 V supplies. The dimensions of the MOS transistors utilized in the MO-CCCCTA architecture are presented in **Table 1**. Firstly, the proposed square-rooting circuit has been simulated to show its workability. **Figure 6** depicts the dc transfer characteristic of the reported square-rooter when the input current I_{in} is swept from 0 to 300 μA along with the variation in bias current I_B from 100 to 200 μA at 50 μA per step. Similarly, **Figure 7** presents the dc transfer characteristics of the designed square-rooter when the bias current I_B is swept from 0 to 300 μA against the vary in input current I_{in} from 50 to 100 μA at 25 μA per step. In these figures, the simulated results are compared with the theoretical values and they are found to be in close agreement over the entire operating range. **Table 2** presents the relative errors of the results in **Figure 6**. The same for the results of **Figure 7** is depicted in **Table 3**.

Figure 8 displays the transient response when a 10 MHz, 150 μA triangular signal is applied to the input of the square rooter for different values of bias current I_B (100, 150 and 200 μA). The same for a 10 MHz, 150 μA sinusoidal signal is shown in **Figure 9**. The frequency response of the proposed square rooter is further investigated and the obtained result is given in **Figure 10**, from which the −3 dB bandwidth is found to be about 445.63 MHz.

Table 1 The dimensions of the MOS transistors utilized in the MO-CCCCTA architecture [27].

Transistor	W/L(μm/μm)
M1, M2	7/0.35
M3, M4	28/0.35
M5-M12	16/0.5
M13-M21	5/0.5
M22, M23	10/0.5
M24-M30	25/0.8
M31-M35	6.2/0.8

Table 2 Theoretical and simulated output currents with percentage errors for the results in **Figure 6**.

I_{IN} (μA)	I_B = 100 μA			I_B = 150 μA			I_B = 200 μA		
	Theoretical	Simulated	% Error	Theoretical	Simulated	% Error	Theoretical	Simulated	% Error
0	0	0.134	-	0	0.157	-	0	0.208	-
50	25	25.245	−0.98	30.618	30.913	−0.96	35.355	35.666	−0.88
100	35.355	35.609	−0.72	43.301	43.574	−0.63	50	49.925	0.15
150	43.301	43.219	0.19	53.033	52.942	0.17	61.237	61.072	0.27
200	50	49.785	0.43	61.237	60.776	0.75	70.711	69.926	1.11
250	55.901	55.298	1.08	68.465	67.855	0.89	79.057	78.219	1.06
300	61.237	60.6	1.04	75	74.175	1.1	86.603	85.633	1.12

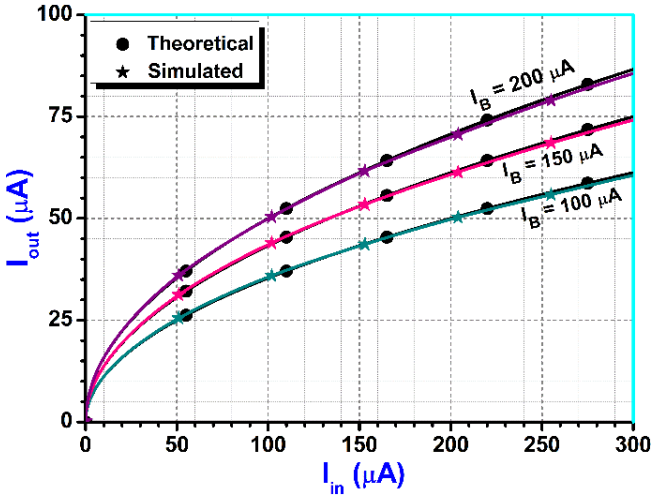

Figure 6 The dc transfer characteristic of the square rooter: Variation of output current I_{out} against input current I_{in}.

Table 3 Theoretical and simulated output currents with percentage errors for the results in **Figure 7**.

I_B (μA)	I_{in} = 50 μA			I_{in} = 75 μA			I_{in} = 100 μA		
	Theoretical	Simulated	% Error	Theoretical	Simulated	% Error	Theoretical	Simulated	% Error
0	0	0	0	0	0	0	0	0	0
50	17.677	17.871	−1.1	21.651	21.855	−0.94	25	25.272	−1.09
100	25	25.245	−0.98	30.619	30.885	−0.87	35.354	35.610	−0.72
150	30.618	30.912	−0.96	37.5	37.8	−0.8	43.301	43.574	−0.63
200	35.356	35.667	−0.88	43.301	43.339	−0.09	50	49.925	0.15
250	39.528	39.951	−1.07	48.412	48.567	−0.32	55.901	55.589	0.56
300	43.301	43.786	−1.12	53.033	53.187	−0.29	61.237	60.717	0.85

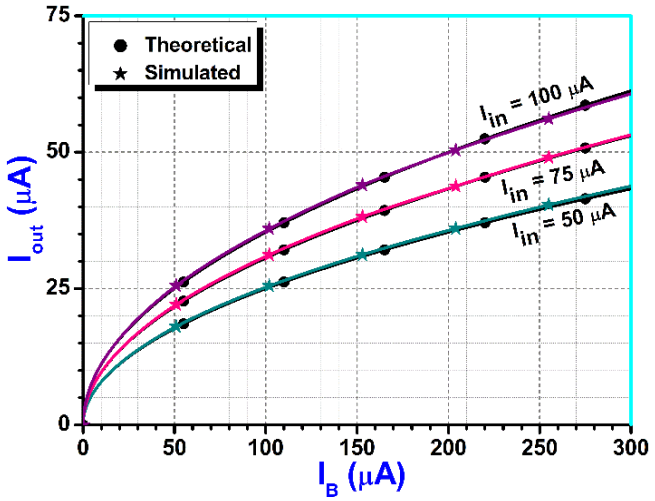

Figure 7 The dc transfer characteristic of the square rooter: Variation of output current I_{out} against bias current I_B.

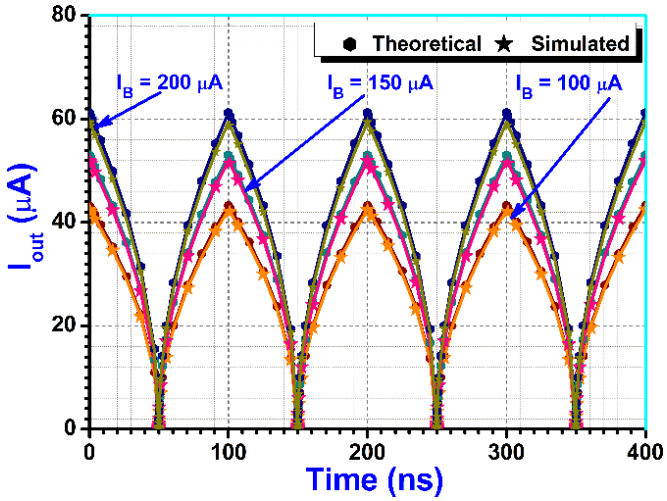

Figure 8 Transient response of the square rooter for triangular input.

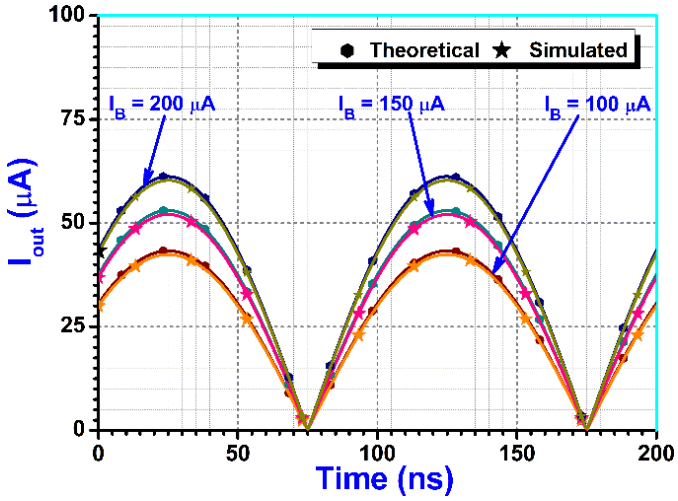

Figure 9 Transient response of the square rooter for sinusoidal input.

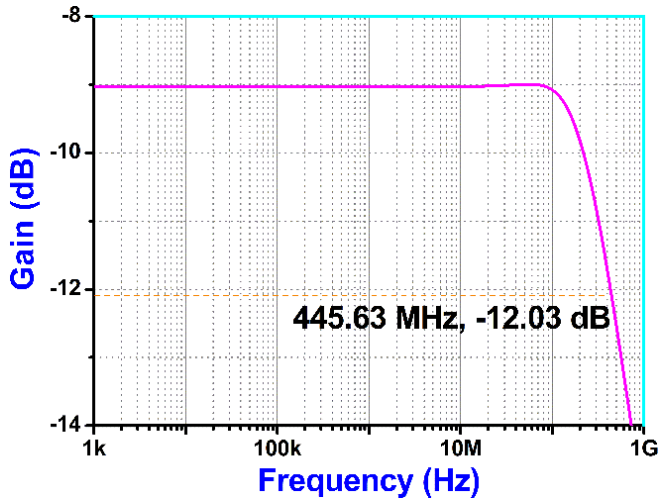

Figure 10 Frequency response characteristic of the designed square-rooter.

The simulation results of the proposed squaring circuits have been given in **Figures 11 - 16**. The variation of output current I_{out} of the squaring circuits reported in **Figures 3** and **4** against the variation of input current I_{in} for different values of bias current I_S are demonstrated in **Figures 11** and **12**, respectively. For both configurations, the input current I_{in} is varied from −300 to 300 µA and the bias current I_S is swept from 50 to 100 µA with increments of 25 µA. Evidently, the squarer of **Figure 4** is a true 4-quadrant squarer while the squarer of **Figure 3** operates only for positive input. This is in accordance with the prediction made earlier in section 'Proposed squaring circuit'. The relative error between the theoretical and simulation outputs for the circuit of **Figure 4** is presented in **Table 4**.

Table 4 Theoretical and simulated output currents with percentage errors for the squarer in **Figure 4**.

I_{IN} (µA)	I_S = 50 µA			I_S = 75 µA			I_S = 100 µA		
	Theoretical	**Simulated**	**% Error**	**Theoretical**	**Simulated**	**% Error**	**Theoretical**	**Simulated**	**% Error**
−300	225	229.815	−2.14	150	152.505	−1.67	112.5	115.178	−2.38
−250	156.25	159.875	−2.32	104.167	106.063	−1.82	78.125	79.953	−2.34
−200	100	102.35	−2.35	66.667	67.32	−0.98	50	51.135	−2.27
−150	56.25	56.959	−1.26	37.5	37.928	−1.14	28.125	28.73	−2.15
−100	25	25.298	−1.19	16.667	16.889	−1.33	12.5	12.788	−2.304
−50	6.25	6.329	−1.26	4.167	4.254	−2.09	3.125	3.199	−2.37
0	0	−0.192	-	0	−0.237	-	0	0.464	-
50	6.25	6.314	−1.02	4.167	4.204	−0.89	3.125	3.193	−2.18
100	25	25.218	−0.87	16.667	16.77	−0.62	12.5	12.688	−1.50
150	56.25	56.576	−0.58	37.5	37.672	−0.46	28.125	28.468	−1.22
200	100	100.35	−0.35	66.667	66.82	−0.23	50	50.275	−0.55
250	156.25	155.125	0.72	104.167	105.052	−0.85	78.125	79.25	−1.44
300	225	222.39	1.16	150	151.56	−1.04	112.5	114.514	−1.79

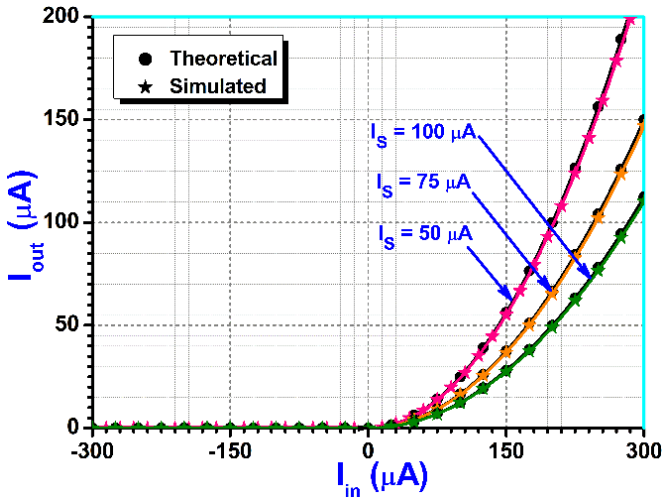

Figure 11 The dc transfer characteristic of the squarer in **Figure 3**.

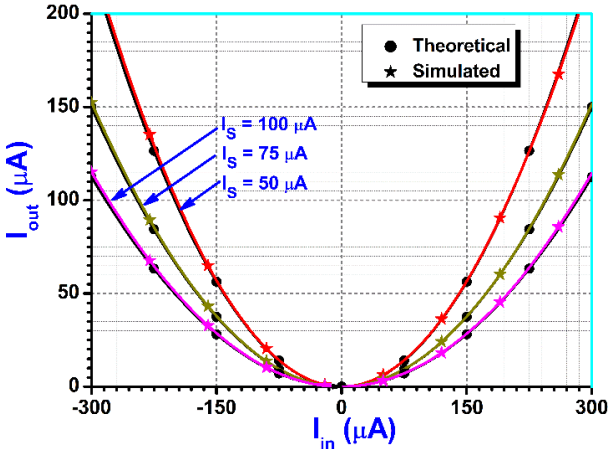

Figure 12 The dc transfer characteristic of the squarer in **Figure 4**.

The gain performance for the squarer in **Figure 4** is further investigated and the result is plotted in **Figure 13**. This is obtained by varying the bias current I_S from 0 to 100 µA and sweeping the input current I_{in} from 150 to 250 µA with 50 µA increment. **Figure 14** shows the frequency response characteristics of the given 4-quadrant squaring circuit, from which the −3 dB bandwidth is calculated as about 61.15 MHz.

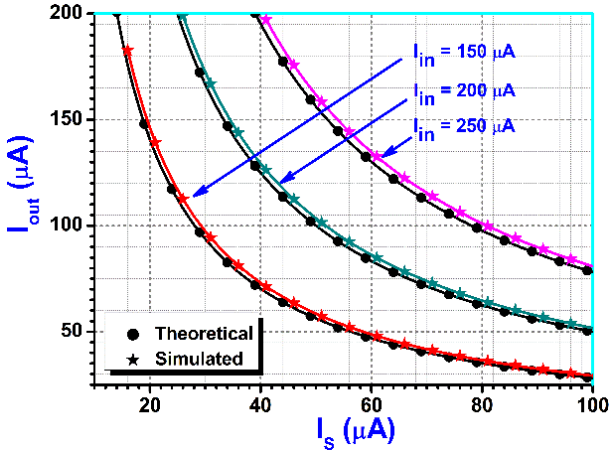

Figure 13 Variation of I_{out} against I_S for the squarer in **Figure 4**.

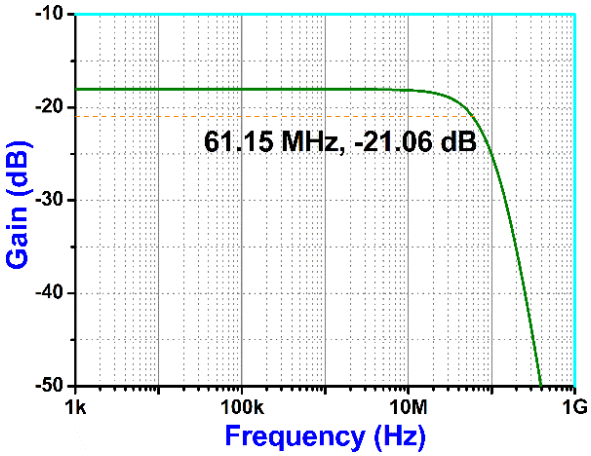

Figure 14 Frequency response characteristic for the squarer in **Figure 4**.

Figure 15 plots the simulated transient response for the current squarer given in **Figure 4**, in which the input current I_{in} is a 10 MHz, 300 µA triangular signal and the bias current I_S is swept from 50 µA to 100 µA with 25 µA increment. In the same manner, the output waveforms generated from the current squarer given in **Figure 4** for a 10 MHz, 300 µA sinusoidal signal is shown in **Figure 16**.

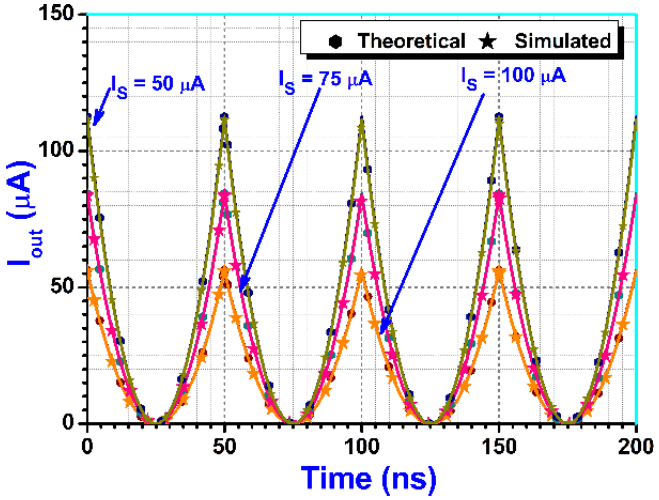

Figure 15 Transient response of the squarer in **Figure 4** for triangular input.

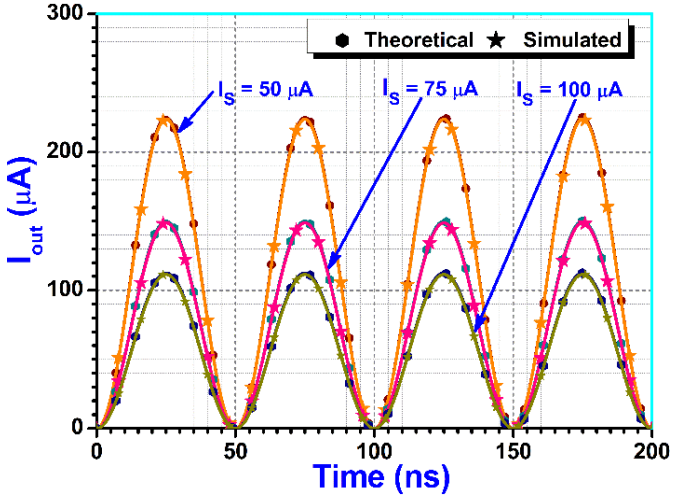

Figure 16 Transient response of the squarer in **Figure 4** for sinusoidal input.

The effects of temperature variation on the output waveforms of the designed square-rooter and current squarer have also been examined by fixing the ambient temperature at 25, 50 and 100 °C. The simulated responses when I_{in} is a 10 MHz, 300 µA triangular signal are presented in **Figures 17** and **18**, respectively. They confirmed that the output performances are insensitive to the temperature variations (maximum deviation is 4.6 % for the squaring circuit for temperature variation from 25 to 100 °C, whereas it is just 0.8 % for the square-rooting circuit). The average power consumption is found to be 0.17 mW and 0.326 mW for the designed square-rooting and 4-quadrant squaring circuit, respectively.

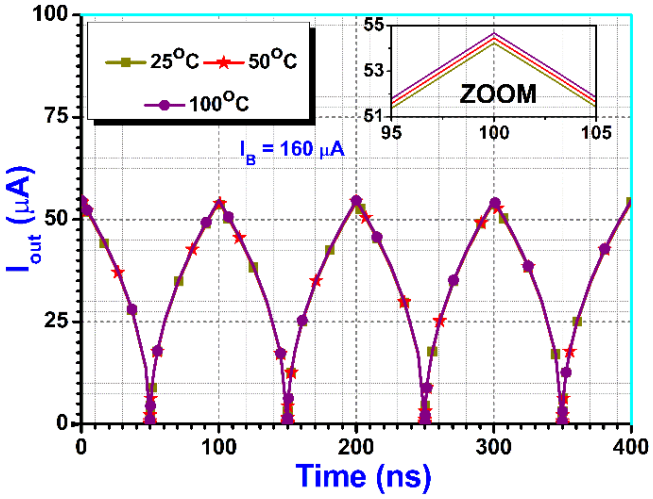

Figure 17 Impact of temperature on output current of the square-rooter.

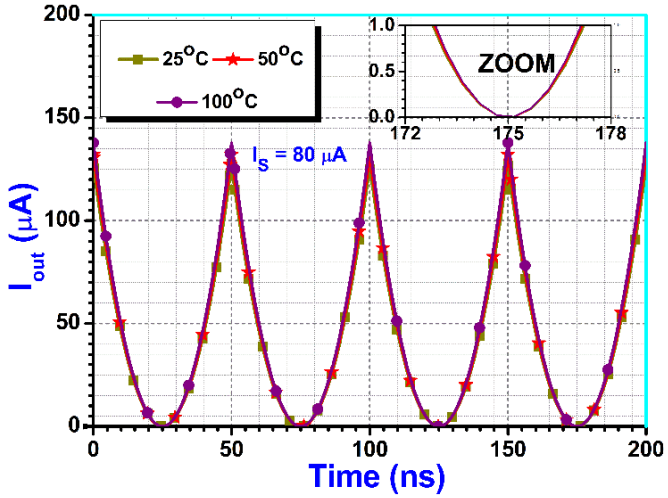

Figure 18 Impact of temperature on output current of the squarer in **Figure 4**.

To verify the robustness of the designed circuits, Monte-Carlo simulations are carried out for hundred runs considering ±5 % deviation in transconductance and threshold voltage of the MOS transistors utilized in the MO-CCCCTA architecture. The simulation outcomes for the measured bandwidth of the proposed square-rooter and 4-quadrant squarer are presented in **Figures 19** and **20**, respectively. Clearly, the −3 dB bandwidth of the square-rooter varies within 441.297 and 449.944 MHz with 1.739 MHz standard deviation whereas the same for the designed 4-quadrant squarer varies within 60.375 and 61.972 MHz with 321.304 kHz standard deviation. The results are satisfactory.

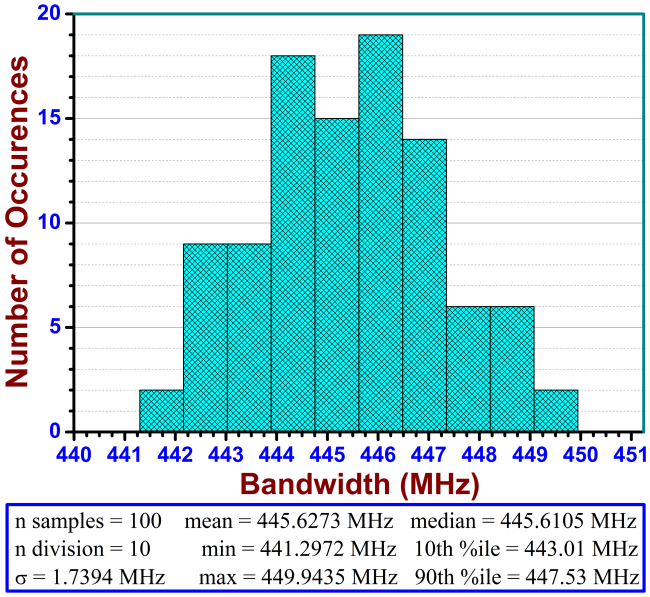

Figure 19 Monte-Carlo simulation outcome for −3 dB bandwidth of the proposed square-rooter.

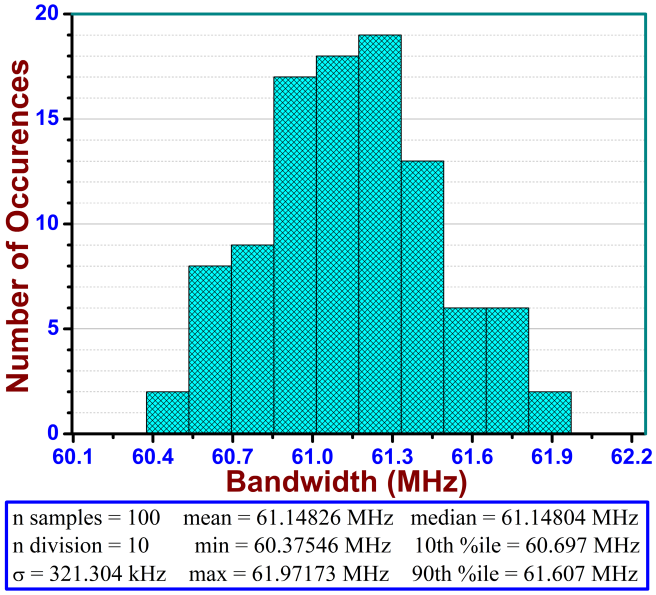

Figure 20 Monte-Carlo simulation outcome for −3 dB bandwidth of the squarer in **Figure 4**.

Application

In order to show the applicability of the reported circuits, a 2-input vector summation circuit is discussed. Vector summation circuit is found extensively useful in many fields like communication, instrumentation and fuzzy systems [6]. Generally, the vector summation computing methods use the squaring and square-rooting function. A possible configuration of 2-input vector summation circuit is depicted in **Figure 21**. Since the designed squaring and square-rooting circuits work with high output impedance, there is no necessity for any intermediate buffer stage. The circuit employs 2 squarer and 1 square-rooter.

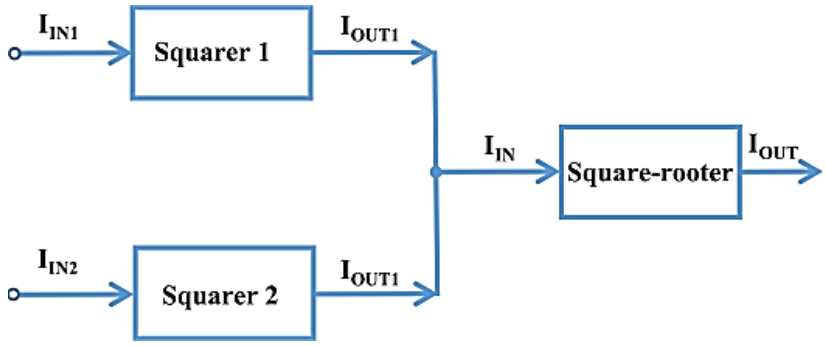

Figure 21 Basic configuration of the 2-input vector summation circuit [6].

The current I_{in_j} has been injected to the j[th] squarer input and then the sum of every single output current I_{out_j} has been applied to the input I_{in} of the square-rooter. Thus;

$$I_{in} = \sum_{j=1}^{2} I_{out_j} \tag{17}$$

Recalling Eqs. (6) and (11), the square-rooter provides the following vector magnitude;

$$I_{out} = k^2 \sqrt{I_B / I_S} \sqrt{I_{in_1}{}^2 + I_{in_2}{}^2} \tag{18}$$

Hence, a 2-input vector summation circuit can be accomplished. **Figure 22** demonstrates the simulated results of the 2-input vector summation circuit employing the proposed squaring and square-rooting circuits. In this case, 2 triangular current signals, one with 300 $\mu A_{p\text{-}p}$ amplitude and 5 MHz frequency and another with 300 $\mu A_{p\text{-}p}$ amplitude and 10 MHz frequency are fed as the input current. The bias currents are set as $I_S = 80\ \mu A$ and $I_B = 200\ \mu A$.

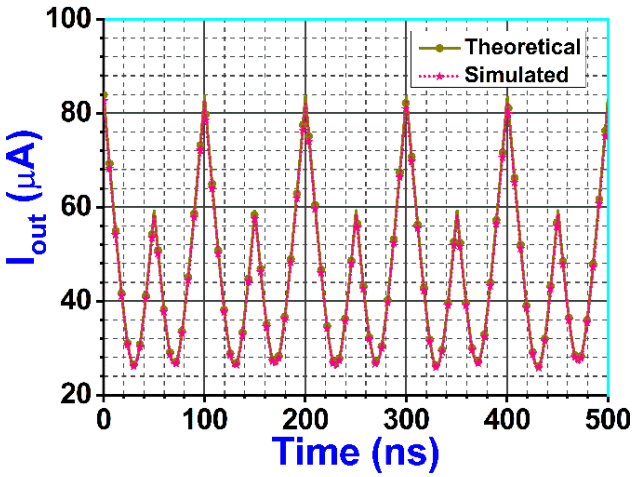

Figure 22 Transient response of the 2-input vector summation circuit.

Discussion and comparison with existing structures

A comparison of the designed current-mode square-rooting and squaring circuits with the previously published active building block based square-rooting and squaring circuits has been demonstrated in **Tables 5** and **6**, respectively. It is clear that the designed square-rooting circuit uses minimum possible components and consumes least power among the references given in **Table 5**. Although the square-rooters of [3,16] provide better linearity than the proposed structure, they needed a very large power supply. Moreover, the bandwidth of the circuits in [3] is very low, while [16] uses a large number of active building blocks. Though the square-rooter of [22] employs only a single active block similar to the proposed structure, it uses bipolar technology, its output impedance is low and also needed a large power supply. Contrarily, the square-rooter of [15] offers larger bandwidth at the cost of poor linearity and additional power dissipation. Evidently, none of the references mentioned in **Table 5** can simultaneously achieve the advantageous features of the proposed square-rooter, i.e., simple architecture, low component count, larger bandwidth, lower power dissipation, electronic tunability, better linearity, insensitivity to temperature drift and availability of high output impedance. Hence, the proposed circuit is strikingly superior to others compared here.

Table 5 Comparison between the suggested and previously reported square-rooting circuits.

Ref. No./ Year	Number and name of active block	Number of active/ passive elements	Output impedance	BW	Power consumption (mW)	Technology	Linearity error	Supply voltage (V)	Mode of operation
[3]/2014	**Figure 3** 1 CDBA, 1B	2 M + 1R	HIGH	3.46 MHz	NR	0.35 µm	< 1 %	±5	Voltage
	Figure 4 1 CDBA	4 M		2.04 MHz			< 2 %		
[4]/2007	**Figure 5** 2 CCCII	3 R	HIGH	60 MHz	50.4	BJT	NR	±2.5	Voltage
	Figure 6 2 CCCII	1 R		12 MHz	5.4				Current
[5]/1995	1 CCII, 2 OP-AMP	2 M + 3 R	LOW	400 kHz	NR	BIC	NR	±6	Voltage
[6]/2010	2 CCCII	-	HIGH	17 MHz	NR	BJT	NR	±1.5	Current
[7]/2013	5 OP-AMP	5R, 2C	LOW	NR	NR	BIC	1.44%	±7.5	Voltage
[8]/2008	2 OP-AMP	7R	LOW	NR	NR	BIC	NR	±12	Voltage
[9]/2017	3 OP-AMP	2 M, 6 R	LOW	NR	NR	BIC	NR	±12	Voltage
[10]/2009	1 OP-AMP	6 R, 1D	LOW	NR	NR	BIC	1.34 %	±12	Voltage
[11]/1992	1 OP-AMP	2 M	LOW	NR	NR	BIC	NR	+5	Trans-impedance
[13]/2017	1 OTRA	3 M	LOW	NR	NR	0.18 µm	NR	±1.5	Voltage
[14]/1996	1 DDCC, - 1 V-I converter	2 M	LOW	NR	NR	CD4007	NR	±7.5	Voltage
[15]/2020	1 OTA, 1B	1 M	HIGH	4.42 GHz	0.442	0.18 µm	< 2.4 %	±0.9	Voltage
[16]/2008	4 OTA	1 R	HIGH	NR	NR	BIC	0.59 %	±15 (max)	Trans-conductance
[17]/1993	3 OTA	2 R	HIGH	NR	NR	BIC	NR	±15 (max)	Voltage
[18]/2010	4 OTA	-	HIGH	163 kHz	NR	BIC	NR	±12	Current
[21]/2011	2 CDTA	-	HIGH	NR	NR	BJT	NR	±3	Current
[22]/2011	1 MO-CTTA	-	LOW	NR	1.83	BJT	NR	±2	Current
[23]/2011	2 MO-CFTA	-	LOW	NR	1.62	BJT	NR	±1.5	Current
[24]/2009	2 CCCDTA	-	HIGH	5.63 MHz	NR	BJT	NR	±1.5	Current
This work	1 MO-CCCCTA	-	HIGH	445.63 MHz	0.17	0.18 µm	≤ 1.12 %	±0.9	Current

D-diode, R-resistance, B-buffer, M-MOSFET, NR- not reported, BW-bandwidth, BIC-bipolar IC, BJT-bipolar junction transistor

Table 6 clearly depicts that of all the circuits the reported squarer operates at low supply voltage, dissipates least power and provides better linearity. Although, [3,4,11,13,14,22] employ less number of active block, but [3,4,11,13,14] needed extra active and/or passive components. Besides, they operate either in voltage or in transconductance mode. On the other hand, [22] is based on bipolar technology and provides low output impedance. Though [6,21] employ the same number of active block as the proposed structure, they are based on bipolar technology. Contrarily, the square of [19] offers larger bandwidth at the cost of poor linearity. Moreover, it employed a large number of active building blocks. Hence, the overall performance of the designed squarer is better than any of the circuits mentioned in **Table 6**, justifying the design proposal.

Table 6 Comparison between the suggested and previously reported squaring circuits.

Ref. No. / Year	Number and name of active block	Number of active/ passive elements	Output impedance	BW	Power consumption (mW)	Linearity error	Supply voltage (V)	Technology	Mode of operation
[3]/2014	1 CDBA	2M, 1R	HIGH	30 MHz	NR	< 2.5 %	±5	0.35 µm	Voltage
[5]/1995	1 CCII	2M, 1R	HIGH	400 kHz	NR	NR	±6	BIC	Voltage
[6]/2010	**Figure 4** 2 CCCII **Figure 5** 3 CCCII	-	HIGH	NR	NR	NR	±1.5	BJT	Current
[11]/1992	1 OP-AMP	4M, 1R	LOW	NR	NR	NR	+5	BIC	Trans-conductance
[12]/2018	1 OTRA	3M	LOW	NR	0.746	NR	±1.5	0.5 µm	Voltage
[14]/1996	1 DDCC	2M	LOW	NR	NR	NR	±7.5	CD4007 CMOS	Trans-conductance
[17]/1993	5 OTA	4R	HIGH	NR	NR	NR	±15 (max)	BIC	Voltage
[19]/2012	4 OTA	1R	LOW	110 MHz	NR	4.8 %	±1.7	BJT	Current
[20]/2020	3 OTA, 1 current squarer	-	LOW	NR	1.2	NR	±1.5	0.25 µm	Voltage
[21]/2011	2 CDTA	-	HIGH	NR	NR	NR	±3	BJT	Current
[22]/2011	1 MO-CTTA	-	LOW	NR	1.83	NR	±2	BJT	Current
[25]/2009	4 CCCDBAs	-	HIGH	NR	6.2	NR	±2	BJT	Current
This work	2 MO-CCCCTA	-	HIGH	61.15 MHz	0.326	≤ 2.38 %	±0.9	0.18 µm	Current

Conclusions

This paper proposes the design of simple current-mode squaring and square-rooting circuits employing MO-CCCCTA as an active block. All the designed circuits consist of only MO-CCCCTA active blocks and do not involve any other external components. They offer attractive features for monolithic IC fabrication due to simple architecture, low component count, electronic tunability, insensitivity to ambient temperature variation (maximum deviation is 4.6 % for the squaring circuit for the temperature variation from 25 to 100 °C, whereas it is just 0.8 % for the square-rooting circuit) and high output impendence. Finally, the applicability of the designed circuits is verified through the implementation of a 2-input vector summation circuit. The simulation results generated through PSPICE software using TSMC 0.18 µm CMOS process parameters show a good agreement with the theoretical analysis. The maximum linearity error in dc transfer characteristic measurement, static power dissipation and the −3 dB bandwidth for the derived square-rooter circuit are 1.12 %, 0.17 mW and 445.63 MHz, respectively. The same for the derived 4-quadrant squaring circuit are 2.38 %, 0.326 mW and 61.15 MHz, respectively. Therefore, the designed circuits definitely excel in others of the same kind and perform way better effectively.

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