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The Modelling of SiC Gate Oxide Thickness based on Thermal Oxidation Temperatures and Durations for High-Voltage Applications

Nuralia Syahida Hashim[1], Banu Poobalan[1,2,*], Nor Farhani Zakaria[1,3], Manikandan Natarajan[4] and Safizan Shaari[1]

[1]Faculty of Electronic Engineering Technology, Universiti Malaysia Perlis, Perlis 02600, Malaysia
[2]MicroSystem Technology, Centre of Excellence, Universiti Malaysia Perlis, Perlis 02600, Malaysia
[3]Advanced Communication Engineering, Centre of Excellence, Universiti Malaysia Perlis, Perlis 02600, Malaysia
[4]Faculty of Dentistry, AIMST University, Kedah 08100, Malaysia

([*]Corresponding author's e-mail: banu@unimap.edu.my)

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Abstract

This research has shown that the oxide thickness for silicon carbide (SiC) based wide materials can be predicted using regression techniques in wet/dry nitrided or wet/dry non-nitrided thermal oxidation process conditions for high voltage applications by employing 2 different regression techniques: Polynomial and linear regression. The R-squared (R^2) and Mean Absolute Percentage Error (MAPE) techniques are used to evaluate the regression models. Furthermore, this work investigates and presents a calculation of gate oxide thickness that is correlated to gate voltage ranges for high voltage applications. In this work, the thermal oxidation process environment is classified into 3 different processing conditions: conventional (dry and wet), dry nitrided (NO,N_2O), and wet nitrided (HNO_3 vapour). The findings from this study showed that wet oxidation combined with nitrided elements can produce thicker and better-quality gate oxide as compared to conventional dry and wet oxidation techniques. The outcome of this work clearly shows that gate oxide thickness may be derived from silicon carbide-based wide-bandgap materials utilizing linear and polynomial approaches using thermal oxidation durations at different temperatures for high-power applications. The regression models and formulations produced in this work are expected to aid the researchers in determining appropriate oxide thickness under practicable process conditions, with the exception of real thermal oxidation process conditions. Hence, the outcome of this work is expected to save the processing time, material, and cost of the power semiconductor device fabrication technology, mainly for high voltage applications.

Keywords: Silicon carbide, Gate oxide thickness, Thermal oxidation, Temperature, Duration, Regression

Introduction

Nowadays, the desire for greater use of natural resources has arisen as a result of the rise in energy consumption in conjunction with technological advancement. Population and technology have an important impact on energy supply and demand. Due to this, using renewable energy sources, which often do not replenish in a human timeframe, has emerged as an appealing option [1]. Power management systems continue to be made possible by power semiconductor devices like power switches and rectifiers. Thyristors, Insulated Gate Bipolar Transistors (IGBTs), and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are a few examples of electronic semiconductor devices that are frequently used to carry out switching in high-power applications [2,3]. For higher voltage applications, including switch-mode power supplies, AC motors, solar inverters, medical and automotive electronics, silicon carbide is often used as an electronic substrate [2-4]. Today, a high-quality, moderately thick gate oxide is needed for high-power technology in order to handle a 15 V of gate voltage (V_G). According to reports, the Fowler-Nordheim tunnelling gate, which is a significant current flow that happens when MOSFETs are operated at high gate voltages, tends to damage the oxide [5,6], especially in thin oxide films [7]. Therefore, a thermally grown thick silicon dioxide (SiO_2) gate with good quality is essential for high-power device applications. Oxides grown on 4H-SiC have been discovered to inherit high interface and near-interface charge densities because of the presence of silicon oxycarbides, carbon clusters, and the incomplete removal of Si-, C-dangling bonds [8-10]. These high charge densities significantly decrease the channel mobility of 4H-Si MOS field-effect transistors, especially near to the conduction-band edge (E_c) [11].

Many researchers are currently attempting to develop thick, reliable, high-quality SiC-based gate oxides. Thermal oxidation in nitrogen-containing gases such as nitrous oxide (N_2O) or nitric oxide (NO) using direct oxidation or post-oxidation annealing (POA) procedures has been reported to improve the SiO_2/SiC interface properties [12-14]. Nevertheless, in order to develop the thick gate oxides, these approaches need a large thermal budget and prolonged processing durations. According to a paper, post-oxidation annealing ambient conditions are less favourable for interfacial carbon removal and nitrogen incorporation at the SiO_2/SiC interface than direct thermal oxidation in NO and N_2O ambient [15]. It has been shown that the presence of nitrogen atoms in strong Si-N bonds aids in the passivation of interface traps resulting from strained and dangling bonds. Additionally, nitrogen atoms create carbon nitrogen (C-N) bonds and release carbon monoxide (CO) [16,17]. However, nitrogen accumulation in the interface region slows the formation of subsequent oxides in SiC, so nitrogen incorporation must be optimized to prevent too much nitrogen from accumulating at the interface region [18,19]. However, oxidation procedures like annealing and growing oxides in diluted N_2O increase the reliability of gate oxides [20]. Nonetheless, the response times are really long. Due to H_2O significantly higher solid solubility in SiO_2 than in O_2, different methods such as developing oxides in wet rather than dry ambient have produced thicker oxides.

Furthermore, hydrogen species have a large influence on the passivation of electrically active defects near the SiO_2/SiC contact [21-23]. Nitrogen [13] and hydrogen [22,23] are found to have a significant influence on improvement in oxide growth in SiO_2/SiC This clarifies the fact that, in thick gate oxide growth under ideal processing conditions for applications involving high power devices, hydrogen and nitrogen play a significant role as passivation species. In this work, gate oxides produced on SiC are classified into 3 processing conditions: Conventional [24-27], dry nitrided, and wet nitrided. Relevant gate oxide thickness developed under various processing conditions is gathered, and carefully examined, and the outcomes are presented in a systematic way. The estimated gate oxide thickness is calculated using regression methods, primarily linear [28] and polynomial [29] regressions, with a range of process lengths and thermal temperatures. This paper also presents the thermal oxidation duration-based regression approach with a range of processing temperatures for high-power applications. Without the need for costly trial work, the models and formulations developed as a result of this work are expected to aid the researchers choose and develop the required oxide thickness under feasible process conditions. The R^2 and MAPE techniques are used to validate the regression models.

Materials and methods

Figure 1 shows the techniques employed in this study to calculate the gate oxide thickness and investigate interface mechanism of gate oxides on SiC. Firstly, the research on SiC-based MOS devices for high-voltage applications, including data gathering and analysis processes, was conducted. The voltage ratings for high-power applications are categorized by the type of application, including power supplies, alternative energy sources, utilities and factory automation. Then, formulas are used to determine the appropriate gate oxide thickness to be formed on the SiC material in accordance with the respective gate voltages.

Three categories of processing approaches were used in this study to generate gate oxide on SiC: standard procedures (dry and wet thermal oxidation process), dry nitridation (NO, N_2O), and wet nitridation (HNO_3) techniques. The conditions for growing gate oxides are further included with various durations and temperatures. The results of numerous experiments are collated and graphs for oxide thickness against processing duration, with respect to different processing temperatures, are presented in this work.

Regression techniques, mostly linear and polynomial regressions, are implied in order to predict the predicted gate oxide thickness with different process durations. $Y = a + bX$, where X is the explanatory variable (duration) and Y is the dependent variable (the thickness of gate oxides), represents a linear regression line and b is the gradient line [30]. The nonlinear relationship between X and Y is modelled by polynomial regression, which uses an equation of the type $Y = 0 + 1X + 2X^2 + ... + hX^h +$, where h is the degree of the polynomial. The relationship with degrees have names (for instance, h = 2 is referred to as quadratic, h = 3 as cubic, and h = 4 as quartic, and so on) [29].

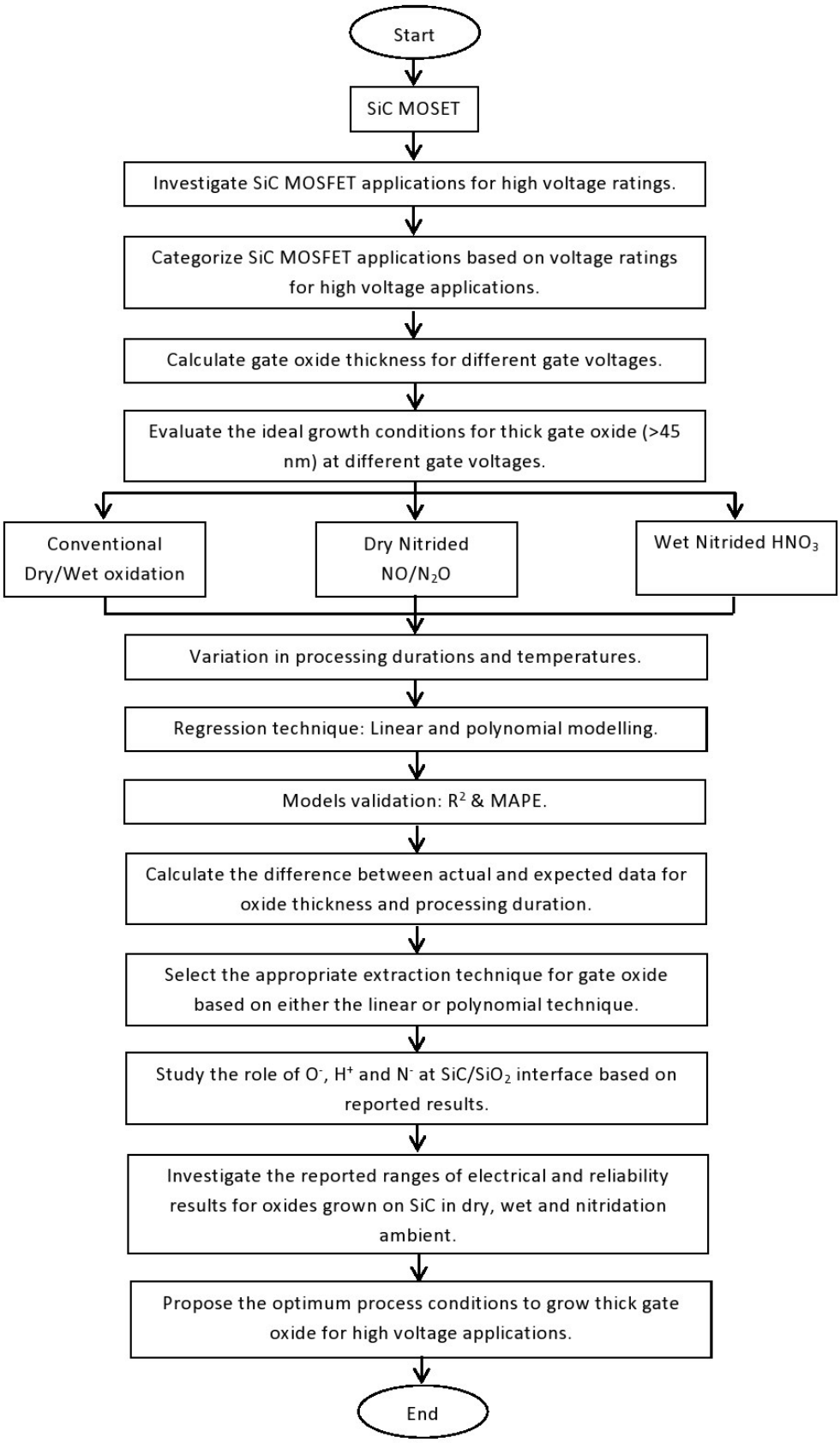

Figure 1 The figure shows the applied procedure on the performance work.

The models and formulations produced as a result of this study are further validated using the R^2 and MAPE techniques. Regression analysis is used to fit the points and create models for the growth of oxides from the graphs. R^2 is a statistical metric that assesses how much variance in a dependent variable is explained by 1 or more independent variables in a regression model [31].

$$R^2 = 1 - \frac{RSS}{TSS} \quad (1)$$

From Eq. (1) RSS and TSS stand for sum of squares of residuals total and sum of squares, respectively, where R^2 denotes coefficient determination. The MAPE is calculated by dividing the total number of absolute errors by the demand (for each individual period). It represents the total of all percentages [32].

$$MAPE = \frac{1}{n}\sum_{t=1}^{n} \left| \frac{A_t - F_t}{A_t} \right| \quad (2)$$

where A_t and F_t are the actual and predicted values, respectively, and n is the number of times the summing iteration occurs. The relationship between oxide thickness and process durations and temperature is evaluated using the R^2 coefficient. The model's dependability is validated using MAPE, as well as the differences between the estimated and real values [33] for process durations.

In addition, studies are also done on the silicon (Si) and carbon (C) reactions to the following elements such as H^+, N^-, O^-. This is followed by the compilation of electrical and reliability results for oxides grown in dry, wet and nitridation ambient on 4H-SiC. Finally, the ideal processing temperature and duration to grow thick gate oxides (> 50 nm) in the most practical conditions for high voltage applications are proposed in this work. The primary purpose of this research is to develop models and formulations to estimate gate oxide thickness in appropriate processing conditions for high-power applications beyond 600 V.

Results and discussion

In **Table 1**, the main uses of SiC-MOSFET in motor controllers and power supplies are listed according to voltage ratings. In order to lower the costs and process steps associated with producing devices, the SiC-based semiconductor industries are aiming for a superior thick SiO_2 gate oxide, particularly for high-voltage applications above 600 V [5,34]. The dielectric constant ratio between oxide and 4H-SiC is shown in Eq. (3) below:

$$\varepsilon_{ratio} = \frac{\varepsilon_{r,SiC}}{\varepsilon_{r,ox}} \quad (3)$$

where the dielectric constants of SiC and oxygen are $\varepsilon_{r,SiC}$ = 10 and ε_r, ox = 3.9, respectively. Eq. (3) implies that during operation, when the device is in the blocking state, the electric field in the gate oxide will be roughly 2.5 times greater than in SiC [5]. The relationship between the electric field in SiC and the gate oxide can be shown using Eq. (4) as follows:

$$E_{SiC} = E_{OX} \left(\frac{\varepsilon_{r,ox}}{\varepsilon_{r,SiC}}\right) \quad (4)$$

The electric field in gate oxide is called E_{ox}, whereas the electric field in silicon carbide is called E_{SiC}. In SiO_2/4H-SiC systems, the maximum surface electric field for SiC, E_{SiC}, must be kept at or below 1.2 MV/cm for safe operational function, which is comparable to 3 MV/cm for the gate oxide, Eox [35]. The electric field is related to gate voltage oxide and gate oxide thickness in shown in Eq. (5) which are further simplified in Eq. (6) as follows:

$$Eox = \frac{(V_G - \phi_{ms})}{\text{tox}} \quad (5)$$

$$t_{ox} = \frac{(V_G - \phi_{ms})}{Eox} \quad (6)$$

Where ϕ_{ms} is the difference in work-function between metal and semiconductor, t_{ox} is the gate oxide thickness, V_G is the gate voltage, and tox is the gate voltage.

Using Eox = 3 MV/cm as the maximum electric field limitation value for 4H-SiC based gate oxide, ϕ_{ms}= 0.45 V, and the requirement for a minimum gate oxide thickness of 50 nm to support gate voltage, a V_G of 15 V is estimated [36]. As the gate voltage is increased, the electric field in the oxide widens, finally causing oxide breakdown [35,37]. It's also important to note that the MOSFET threshold voltage increases with oxide layer thickness [7]. Therefore, it is essential to thermally develop a thick SiO_2 gate (> 50 nm) with great quality for high-power devices. Therefore, it is essential to thermally develop a thick SiO_2 gate (> 50 nm) with good quality for high-power devices. The majority of SiC-based power devices for high voltage applications operate safely at voltage ratings between 15 and 18 V. According to the gate voltage used, **Table 2** shows the gate oxide thickness required for high power applications using Eq. (6).

Table 1 The main applications of SiC-MOSFETs in motor controls and power supplies [38].

Uses of SiC-MOSFET	Voltage Rating (v)
Resident appliance (air conditioners, freezer, clothes dryers)	600 V
Power electrical train	500 - 1000 V
Electric transportation charger	600 - 1200 V
Photovoltaic inverters, wind farms	1 - 6.5 kV

Table 2 The requirement for gate oxide thickness estimation is based on gate voltages for high power applications.

The gate oxide thickness estimation, T_{ox} (nm)	Gate voltage, V_G (V)
48.5	15
51.8	16
55.1	17
58.5	18

Table 3 Modeling of process conditions to grow gate oxides with varied temperatures and durations using regression (R^2) (Linear) techniques.

Gate Voltages (V)	Estimated Oxide Thickness (nm)	Process Temperature (°C)	Process Conditions	Actual Process Duration (Hour)	Calculated Process Duration (Hour)	Calculated and Actual process duration difference (%)	Tox percentage difference (%)	Model Formula	R^2	MAPE (%)	Process Conditions	Actual Process Duration (Hour)	Calculated Process Duration (Hour)	Calculated and Actual process duration difference (%)	Tox percentage difference (%)	Model Formula	R^2	MAPE (%)
15	48.5	1000	Wet	NA	14.18	NA	0.02	y=2.9212x+7.0858	0.9961	2.10	Dry	NA	16.64	NA	0.02	y=2.6289x+4.768	0.9257	20.66
		1050		NA	7.85	NA	0.00	y=5.2062x+7.6289	0.9699	6.38		NA	15.82	NA	0.02	y=2.7072x+5.667	0.9332	15.22
		1100		4.38	4.14	5.48	0.02	y=8.9938x+11.271	0.9359	8.26		NA	7.23	NA	0.04	y=4.96x+12.62	0.9632	7.24
		1150		2.92	2.49	14.73	0.02	y=9.2355x+25.512	0.9451	4.73		3.76	3.92	4.26	0.02	y=7.4289x+19.368	0.9810	5.03
16	51.8	1000		NA	15.31	NA	0.02	y=2.9212x+7.0858	0.9961	2.10		NA	17.89	NA	0.00	y=2.6289x+4.768	0.9257	20.66
		1050		NA	8.48	NA	0.04	y=5.2062x+7.6289	0.9699	6.38		NA	17.04	NA	0.00	y=2.7072x+5.667	0.9332	15.22
		1100		4.45	4.51	1.35	0.06	y=8.9938x+11.271	0.9359	8.26		NA	7.90	NA	0.00	y=4.96x+12.62	0.9632	7.24
		1150		3.08	2.85	7.47	0.06	y=9.2355x+25.512	0.9451	4.73		4.20	4.37	4.05	0.06	y=7.4289x+19.368	0.9810	5.03
17	55.1	1000		NA	16.44	NA	0.02	y=2.9212x+7.0858	0.9961	2.10		NA	19.15	NA	0.02	y=2.6289x+4.768	0.9257	20.66
		1050		NA	9.12	NA	0.02	y=5.2062x+7.6289	0.9699	6.38		NA	18.26	NA	0.00	y=2.7072x+5.667	0.9332	15.22
		1100		4.62	4.87	5.41	0.06	y=8.9938x+11.271	0.9359	8.26		NA	8.56	NA	0.04	y=4.96x+12.62	0.9632	7.24
		1150		3.30	3.20	3.03	0.06	y=9.2355x+25.512	0.9451	4.73		4.59	4.81	4.79	0.00	y=7.4289x+19.368	0.9810	5.03
18	58.5	1000		NA	17.60	NA	0.00	y=2.9212x+7.0858	0.9961	2.10		NA	20.44	NA	0.00	y=2.6289x+4.768	0.9257	20.66
		1050		NA	9.77	NA	0.00	y=5.2062x+7.6289	0.9699	6.38		NA	19.52	NA	0.02	y=2.7072x+5.667	0.9332	15.22
		1100		4.82	5.25	8.92	0.02	y=8.9938x+11.271	0.9359	8.26		NA	9.25	NA	0.00	y=4.96x+12.62	0.9632	7.24
		1150		3.42	3.57	4.39	0.03	y=9.2355x+25.512	0.9451	4.73		5.10	5.27	3.33	0.03	y=7.4289x+19.368	0.9810	5.03
15	48.5	1050	N_2O	NA	53.89	NA	0.00	y=0.9x-2E-15	1	0	NO	NA	121.25	NA	0.00	y=0.4x	1	0
		1100		NA	13.86	NA	0.02	y=3.5x	1	0		NA	53.89	NA	0.00	y=0.9x-2E-15	1	0
		1150		NA	8.08	NA	0.04	y=6x	1	0		NA	12.13	NA	0.04	y=4x	1	0
		1175		NA	6.93	NA	0.02	y=7x	1	0		NA	9.70	NA	0.00	y=5x	1	0
16	51.8	1050		NA	57.56	NA	0.00	y=0.9x-2E-15	1	0		NA	129.50	NA	0.00	y=0.4x	1	0
		1100		NA	14.80	NA	0.00	y=3.5x	1	0		NA	57.56	NA	0.00	y=0.9x-2E-15	1	0
		1150		NA	8.63	NA	0.04	y=6x	1	0		NA	12.95	NA	0.00	y=4x	1	0
		1175		NA	7.40	NA	0.00	y=7x	1	0		NA	10.36	NA	0.00	y=5x	1	0
17	55.1	1050		NA	61.22	NA	0.00	y=0.9x-2E-15	1	0		NA	137.75	NA	0.00	y=0.4x	1	0
		1100		NA	15.74	NA	0.02	y=3.5x	1	0		NA	61.22	NA	0.00	y=0.9x-2E-15	1	0
		1150		NA	9.18	NA	0.04	y=6x	1	0		NA	13.78	NA	0.04	y=4x	1	0
		1175		NA	7.87	NA	0.02	y=7x	1	0		NA	11.02	NA	0.00	y=5x	1	0
18	58.5	1050		NA	65.00	NA	0.00	y=0.9x-2E-15	1	0		NA	146.25	NA	0.00	y=0.4x	1	0
		1100		NA	16.71	NA	0.02	y=3.5x	1	0		NA	65.00	NA	0.00	y=0.9x-2E-15	1	0
		1150		NA	9.75	NA	0.00	y=6x	1	0		NA	14.63	NA	0.03	y=4x	1	0
		1175		NA	8.36	NA	0.03	y=7x	1	0		NA	11.70	NA	0.00	y=5x	1	0
15	48.5	1000	Direct HNO_3	NA	NA	NA	NA	NA	NA	NA	POA HNO_3	NA	NA	NA	NA	NA	NA	NA
		1050		NA	6.83	NA	0.04	y=6x+7.5	0.9231	8.00		2.70	2.70	0.00	0.04	y=14.5x+9.3333	0.9372	7.70
		1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
16	51.8	1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1050		NA	7.38	NA	0.04	y=6x+7.5	0.9231	8.00		2.84	2.93	3.17	0.04	y=14.5x+9.3333	0.9372	7.70
		1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
17	55.1	1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1050		NA	7.93	NA	0.04	y=6x+7.5	0.9231	8.00		3.02	3.16	4.63	0.09	y=14.5x+9.3333	0.9372	7.70
		1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
18	58.5	1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1050		NA	8.50	NA	0.00	y=6x+7.5	0.9231	8.00		NA	3.39	NA	0.02	y=14.5x+9.3333	0.9372	7.70
		1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA

Table 4 Modeling of process conditions to grow gate oxides with varied temperatures and durations using regression (R^2) (Polynomial) techniques.

Gate Voltages (V)	Estimated Oxide Thickness (nm)	Process Temperature (°C)	Process Conditions	Actual Process Duration (Hour)	Calculated Process Duration (Hour)	Calculated and Actual process duration difference (%)	Tox percentage difference (%)	Model Formula	R^2	MAPE (%)	Process Conditions	Actual Process Duration (Hour)	Calculated Process Duration (Hour)	Calculated and Actual process duration difference (%)	Tox percentage difference (%)	Model Formula	R^2	MAPE (%)
		1000		NA	8.64	NA	0.02	y = 0.0306x4-0.436x3+2.139x2-1.1126x+9.0835	0.9994	1.53		NA	11.73	NA	0.02	y = 0.0748x3 - 1.1512x2 + 7.2851x + 0.69	0.9983	2.69
		1050		NA	6.78	NA	0.00	y = 0.003x4-0.3448x3+3.3529x2-4.1057x+13.333	0.9880	3.14		NA	11.44	NA	0.00	y = 0.076x3 - 1.1517x2 + 7.3214x + 1.653	0.9990	1.62
15	48.5	1100		4.38	4.34	1.03	0.00	y = -0.8341x4+11.233x3-49.532x2+86.663x-16.891	0.9941	2.38		NA	7.02	NA	0.00	y = 0.1218x3 - 1.4316x2 + 9.6503x + 9.1904	0.9732	4.75
		1150		2.92	2.65	9.28	0.00	y=-0.1155x4+0.8711x3-0.6931x2+5.867x+27.316	0.9786	3.48		3.76	3.68	2.15	0.00	y = -0.0405x4 + 0.4356x3 - 1.9191x2 + 12.211x + 15.282	0.9982	1.38
		1000		NA	8.83	NA	0.02	y = 0.0306x4-0.436x3+2.139x2-1.1126x+9.0835	0.9994	1.53		NA	12.02	NA	0.00	y = 0.0748x3 - 1.1512x2 + 7.2851x + 0.69	0.9983	2.69
		1050		NA	6.92	NA	0.00	y = 0.003x4-0.3448x3+3.3529x2-4.1057x+13.333	0.9880	3.14		NA	11.74	NA	0.00	y = 0.076x3 - 1.1517x2 + 7.3214x + 1.653	0.9990	1.62
16	51.8	1100		4.45	4.51	1.30	0.00	y = -0.8341x4+11.233x3-49.532x2+86.663x-16.891	0.9941	2.38		NA	7.43	NA	0.00	y = 0.1218x3 - 1.4316x2 + 9.6503x + 9.1904	0.9732	4.75
		1150		3.08	2.92	5.26	0.00	y=-0.1155x4+0.8711x3-0.6931x2+5.867x+27.316	0.9786	3.48		4.20	4.14	1.43	0.02	y = -0.0405x4 + 0.4356x3 - 1.9191x3 + 12.211x + 15.282	0.9982	1.38
		1000	Wet	NA	8.99	NA	0.04	y=0.0306x4-0.436x3+2.139x2-1.1126x+9.0835	0.9994	1.53	Dry	NA	12.28	NA	0.02	y = 0.0748x3 - 1.1512x2 + 7.2851x + 0.69	0.9983	2.69
		1050		NA	7.06	NA	0.00	y = 0.003x4-0.3448x3+3.3529x2-4.1057x+13.333	0.9880	3.14		NA	12.01	NA	0.02	y = 0.076x3 - 1.1517x2 + 7.3214x + 1.653	0.9990	1.62
17	55.1	1100		4.62	4.68	1.28	0.00	y = -0.8341x4+11.233x3-49.532x2+86.663x-16.891	0.9941	2.38		NA	7.79	NA	0.00	y = 0.1218x3 - 1.4316x2 + 9.6503x + 9.1904	0.9732	4.75
		1150		3.30	3.17	0.46	0.00	y=-0.1155x4+0.8711x3-0.6931x2+5.867x+27.316	0.9786	3.48		4.59	4.60	0.17	0.00	y = -0.0405x4 + 0.4356x3 - 1.9191x2 + 12.211x + 15.282	0.9982	1.38
		1000		NA	9.15	NA	0.02	y = 0.0306x4-0.436x3+2.139x2-1.1126x+9.0835	0.9994	1.53		NA	12.54	NA	0.00	y = 0.0748x3 - 1.1512x2 + 7.2851x + 0.69	0.9983	2.69
18	58.5	1050		NA	7.19	NA	0.00	y = 0.003x4-0.3448x3+3.3529x2-4.1057x+13.333	0.9880	3.14		NA	12.27	NA	0.00	y = 0.076x3 - 1.1517x2 + 7.3214x + 1.653	0.9990	1.62
		1100		4.82	4.86	0.85	0.00	y = -0.8341x4+11.233x3-49.532x2+86.663x-16.891	0.9941	2.38		NA	8.13	NA	0.00	y = 0.1218x3 - 1.4316x2 + 9.6503x + 9.1904	0.9732	4.75
		1150		3.42	3.43	0.41	0.00	y= -0.1155x4+0.8711x3-0.6931x2+5.867x+27.316	0.9786	3.48		5.10	5.20	1.86	0.00	y = -0.0405x4 + 0.4356x3 - 1.9191x2 + 12.211x + 15.282	0.9982	1.38
		1050		NA	53.889	NA	0.000	y=0.9x-1E-14	1	0		NA	121.250	NA	0.000	y=4E-16x2+0.4x-5E-15	1	0
		1100		NA	13.857	NA	0.000	y=3.5x-7E-14	1	0		NA	53.889	NA	0.000	y=0.9x-1E-14	1	0
15	48.5	1150		NA	8.083	NA	0.000	y=7E-15x2+6x-8E-14	1	0		NA	12.125	NA	0.000	y=4x-7E-14	1	0
		1175		NA	6.929	NA	0.000	y=7x-1E-13	1	0		NA	9.700	NA	0.000	y=5x-9E-14	1	0
		1050		NA	57.556	NA	0.000	y=0.9x-1E-14	1	0		NA	129.500	NA	0.000	y=4E-16x2+0.4x-5E-15	1	0
		1100		NA	14.800	NA	0.000	y=3.5x-7E-14	1	0		NA	57.556	NA	0.000	y=0.9x-1E-14	1	0
16	51.8	1150		NA	8.633	NA	0.000	y=7E-15x2+6x-8E-14	1	0		NA	12.950	NA	0.000	y=4x-7E-14	1	0
		1175	N_2O	NA	7.400	NA	0.000	y=7x-1E-13	1	0	NO	NA	10.360	NA	0.000	y=5x-9E-14	1	0
		1050		NA	61.222	NA	0.000	y=0.9x-1E-14	1	0		NA	137.750	NA	0.000	y=4E-16x2+0.4x-5E-15	1	0
		1100		NA	15.743	NA	0.000	y=3.5x-7E-14	1	0		NA	61.222	NA	0.000	y=0.9x-1E-14	1	0
17	55.1	1150		NA	9.183	NA	0.000	y=7E-15x2+6x-8E-14	1	0		NA	13.775	NA	0.000	y=4x-7E-14	1	0
		1175		NA	7.871	NA	0.000	y=7x-1E-13	1	0		NA	11.020	NA	0.000	y=5x-9E-14	1	0
		1050		NA	65.000	NA	0.000	y=0.9x-1E-14	1	0		NA	146.250	NA	0.000	y=4E-16x2+0.4x-5E-15	1	0
		1100		NA	16.714	NA	0.000	y=3.5x-7E-14	1	0		NA	65.000	NA	0.000	y=0.9x-1E-14	1	0
18	58.5	1150		NA	9.750	NA	0.000	y=7E-15x2+6x-8E-14	1	0		NA	14.625	NA	0.000	y=4x-7E-14	1	0
		1175		NA	8.357	NA	0.000	y=7x-1E-13	1	0		NA	11.700	NA	0.000	y=5x-9E-14	1	0
		1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1050		NA	4.123	NA	0.000	y=-3x2+18x-2.5	1	0		2.700	2.749	1.810	0.020	y=6.5x2-11.5x+31	1	0
15	48.5	1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1050		NA	4.254	NA	0.000	y=-3x2+18x-2.5	1	0		2.840	2.880	1.410	0.020	y=6.5x2-11.5x+31	1	0
16	51.8	1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150	Direct HNO_3	NA	NA	NA	NA	NA	NA	NA	POA HNO_3	NA	NA	NA	NA	NA	NA	NA
		1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1050		NA	4.382	NA	0.000	y=-3x2+18x-2.5	1	0		3.020	3.004	0.530	0.020	y=6.5x2-11.5x+31	1	0
17	55.1	1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1000		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	Na	NA
18	58.5	1050		NA	4.509	NA	0.000	y=-3x2+18x-2.5	1	0		NA	3.124	NA	0.020	y=6.5x2-11.5x+31	1	0
		1100		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA
		1150		NA	NA	NA	NA	NA	NA	NA		NA	NA	NA	NA	NA	NA	NA

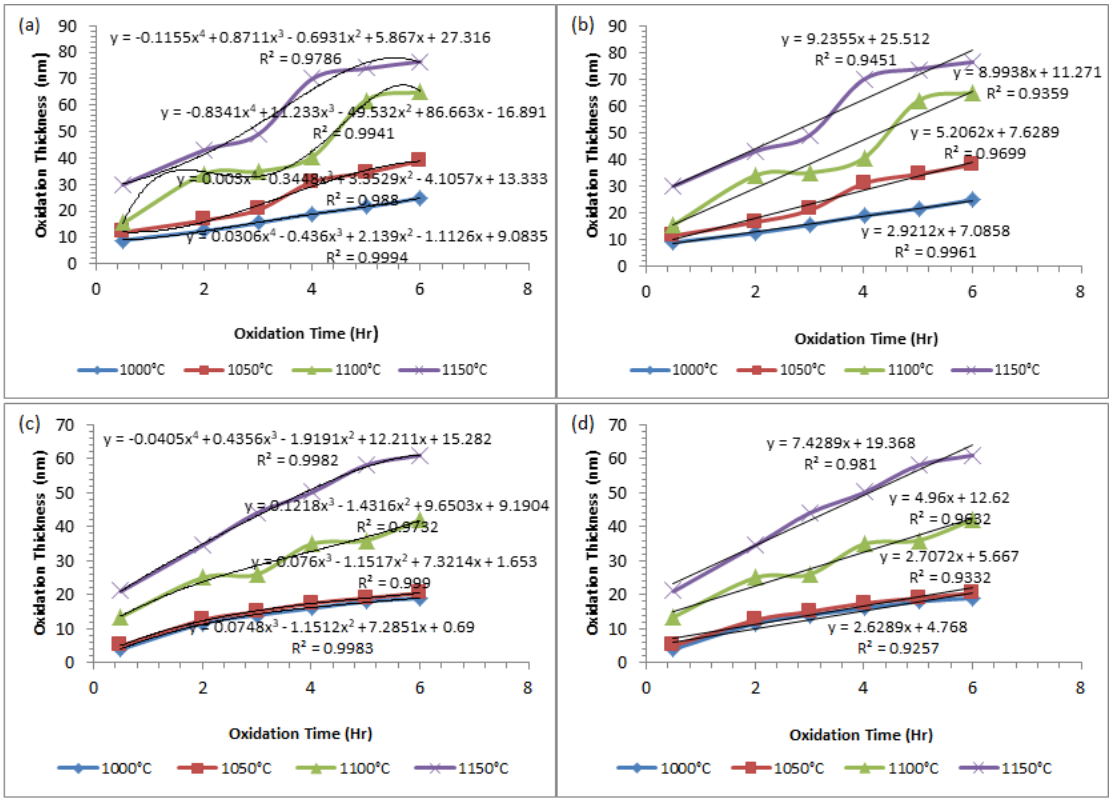

Figure 2 The graph of the SiC oxide development profile using polynomial and linear regression (a) Polynomial N_2O, (b) Linear N_2O, (c) Polynomial NO and (d) Linear NO.

The graphs for oxide thickness against processing duration in relation to different processing temperatures are shown in **Figure 2**. Regression analysis is used to predict the gate oxide thickness corresponding to the gate voltages calculated in **Table 2** for high power applications. The gate oxide thickness is extracted based on the collected data [6]. Both linear and polynomial regressions are utilized to evaluate the desired gate oxide thickness based on the gate voltages. Predictive modelling demonstrates that polynomial regression offers more accurate and better fitting than linear regression, which is further supported by the low value of 5 % MAPE for dry and wet oxidation using polynomial regression approaches. Through using a linear regression approach, the MAPE values for wet and dry oxidation are 10 and 21 %, respectively. The substantial correlation between oxide thickness and oxidation duration was further confirmed by the higher R_2 (> 0.9) value for both linear and polynomial regression. This was further validated by the fact that the value was more accurately adjusted for polynomial than linear regression.

Additionally, it is noted that the percentage difference between actual and calculated duration when using linear regression is less than 5 % for dry and less than 15 % for wet oxidation, and the percentage difference when using polynomial regression is less than 5 % for dry and 10 % for wet oxidation. Predictive modelling demonstrates that polynomial regression offers more accurate and better fitting than linear regression, which is further supported by the low value < 5 % of MAPE for dry and wet oxidation using polynomial regression approaches. Using the linear regression approach, the MAPE values for wet and dry oxidation are < 10 % and < 21 %, respectively. Furthermore, the analysis produces a formulation that can be used as predictive modelling for the extraction of gate oxide thickness at high power gate voltages. **Tables 3** and **4** present the formulation and findings for dry and wet oxidation processing conditions using different durations and different temperatures. In polynomial and linear regression, the thickness difference between estimated and actual values is less than 0.04 % and less than 0.06 %, respectively. This proves that the polynomial regression method, which offers superior fitting to linear regression, can be used in dry and wet oxidation situations for a variety of thermal durations and temperatures. Even though the increase in temperature and duration results in thicker gate oxide, it is seen that the effect of temperature is more significant since its oxide growth rate is faster than the counterpart associated with duration.

Figure 2 shows that the oxide growth rises with temperature and duration, with wet oxidation showing a larger increase than dry oxidation. The figures show that growing oxides in wet oxidation, as opposed to

dry oxidation, leads to thicker oxide layers because H_2O has a far larger solid solubility in SiO_2 than in O_2 [36,38,39]. Likewise, it has been observed that the rate of wet oxidation slows down after 5 h. This is due to the fact that when oxide thickness rises, H_2O penetrating into the existing oxide becomes slower and then results in a limitation on further oxidation rate. Furthermore, wet oxidation is anticipated to result in hydrogen passivation of electrically active defects near the SiO_2/SiC interface [6,39,40].

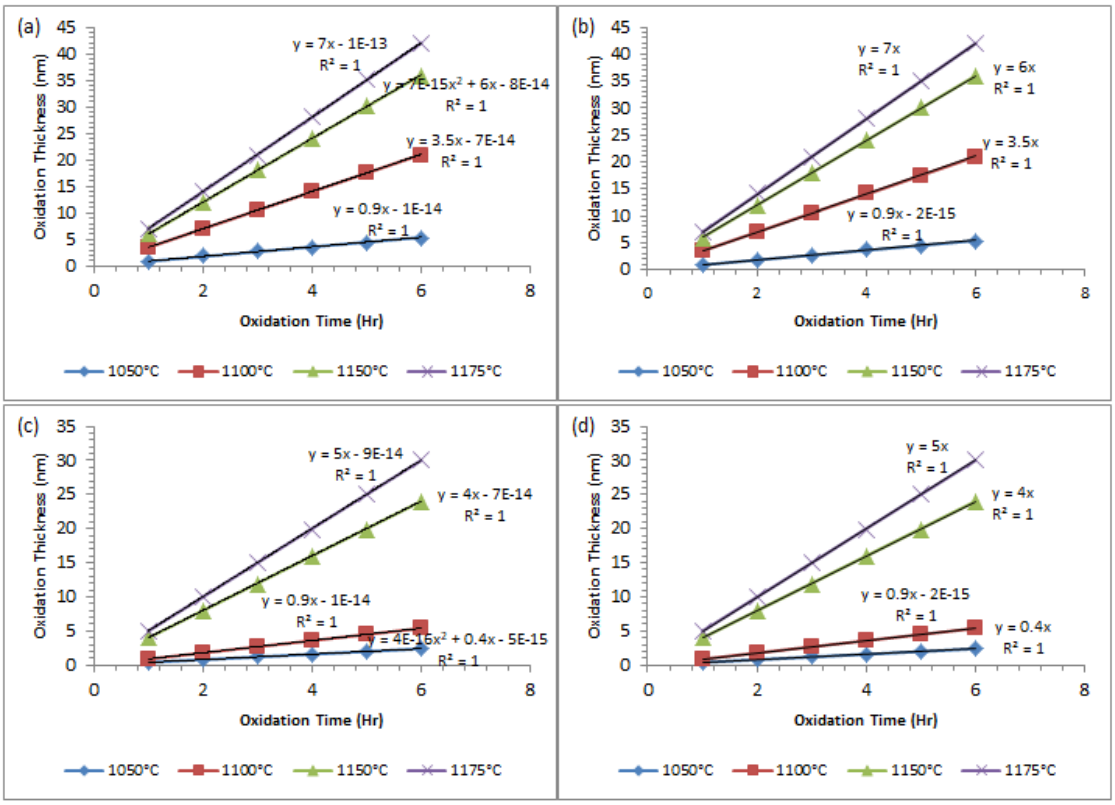

Figure 3 The graph of the SiC oxide development profile using polynomial and linear regression (a) Polynomial N_2O, (b) Linear N_2O, (c) Polynomial NO, (d) Linear NO.

Figure 3 shows the estimated and displayed oxide growth profile on the Si-face by dry N_2O and NO nitridation. Nitridated oxide is observed to have less thickness than traditional (dry and wet) oxidation in terms of the growth rate. The Si-N bonds at the interface, which lead to a decrease in the concentration of growth sites, may be a contributing factor in the decreased thickness. According to Gupta and Akhtar [6] and Chanthaphan *et al.* [41], there are 2 sets of mechanisms at the SiO_2/SiC interface that are said to be affected by nitridation: (1) the formation of strong SiN bonds that passivate interface traps caused by dangling and strained bonds, and (2) the elimination of carbon. Under both conditions, the creation of these bonds increases the gate-oxide dependability while simultaneously dramatically lowering the initial interface-trap density. This is because the much stronger SiN bond energy levels are outside of the SiC energy gap, making them electrically passive defects [19,42].

The majority of the CO, carbon dioxide (CO_2) or CN molecules formed during the oxidation diffuse out of the oxide when the second function of nitridation, which is connected to the removal of carbon from the interface, is taken into consideration. The development of complex silicon oxycarbon compounds at the interface is caused by some of the carbon atoms' tendency to concentrate as carbon clusters and act as interface traps [43]. It has been observed that in an N_2O environment, oxides grow more quickly than in a NO environment. According to one study, NO annealing causes significantly less (carbon-carbon) C-C graphitization than N_2O post-oxidation treatment [41-43]. Carbon atoms aggregate into carbon clusters as the oxide layer rises, eventually increasing the interface traps. This confirms that the rate of oxidation in N_2O is significantly higher than that of the ambient NO, which explains the increased concentration of carbon clusters near the interface [44,45]. Moreover, because the fitting is based on Arrhenius plots for linear oxide growth in NO and N_2O, the R^2 and MAPE values for this group of studies show 1 and 0

respectively. It is noted that for the linear regression and the polynomial regression methods, the thickness difference between estimated and actual values is less than 0.1 and 0 %, respectively.

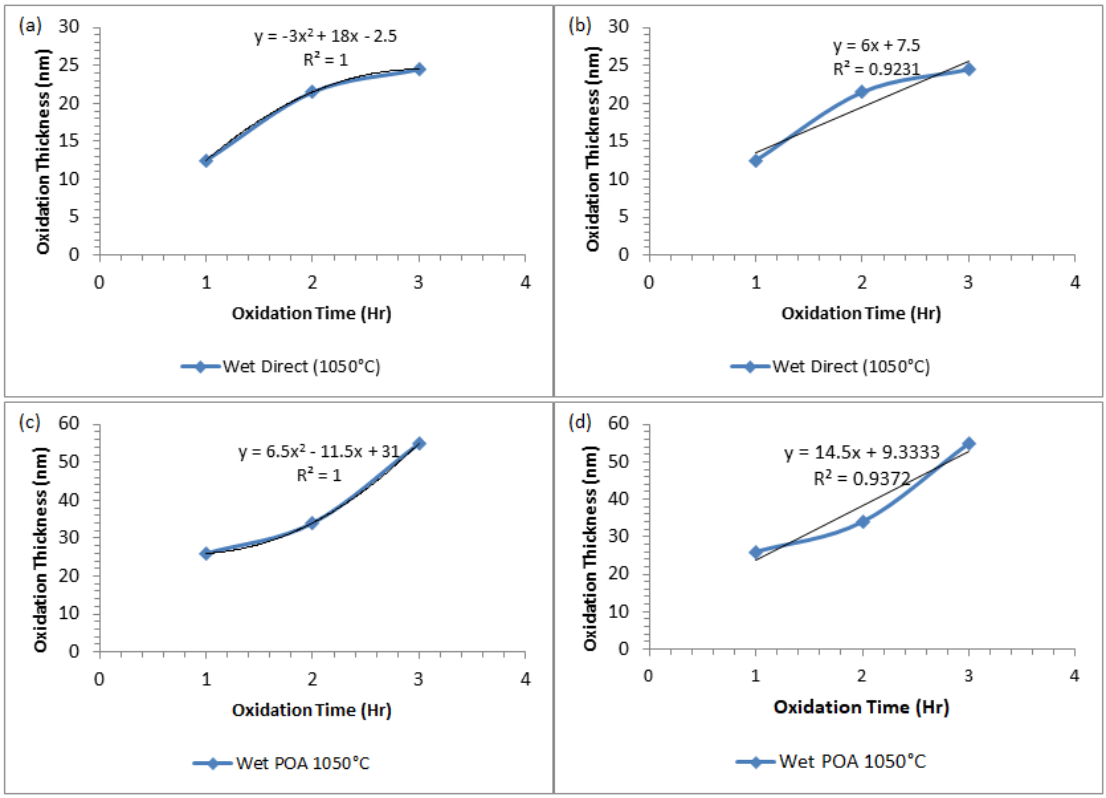

Figure 4 The graph of oxide growth profile on SiC by Linear/ Polynomial Regression (a) Polynomial Direct HNO_3, (b) Linear Direct HNO_3, (c) Polynomial POA HNO_3, (d) Linear POA HNO_3.

Wet nitridation has been achieved by using nitric acid in direct and post oxidation annealing, combining the benefits of nidridation processes in a wet environment [21,46] as shown in **Figure 4**. Gate oxide thickness is thicker in samples treated under wet nitration conditions than under other circumstances. The oxidation rate is significantly higher when HNO_3 and H_2O vapour are used together during oxidation than when H_2O vapour is used alone [15,20,47]. Hydrogen peroxide (H_2O_2) and H_2O passivate Si and C dangling bonds more quickly than dry oxidation and passivate oxycarbide bonds. However, a combination of H and N elements, such as NH_3, passivates and eliminates C-related defects and dangling bonds without causing the oxide layer to oxidise. N_2O and NO passivate Si dangling bonds and eliminate oxycarbides linkages. However, too much nitrogen accumulation at the interface tends to lower the growth site concentration [20,48].

As can be seen from **Tables 3** and **4**, polynomial regression offers better fitting than linear regression, with a larger R^2 and a lower MAPE value, respectively. When utilizing the linear regression approach, it is seen that MAPE is below 10 % and R^2 is above 0.9 for wet nitridation oxidation. In contrast, it appears that R^2 is 1 and MAPE is 0 % for wet nitridation models using the polynomial regression fitting approach, which shows good fitting. For Wet POA HNO_3, the difference in thickness between calculated and actual is less than 0.1 %, while the difference in duration between actual and calculated is less than 5 % using the linear regression approach. On the other hand, the thickness difference between calculated and actual for the Wet POA HNO_3 group utilizing the polynomial regression approach is less than 0.02 %, whereas the percentage of duration difference between actual and calculated for that group is less than 2 %.

Table 5 summarizes the C and Si reactions at the SiO_2/SiC interface during oxidation under dry and wet oxidation techniques. This demonstrates that H^+ aids in the passivation of Si and C [49,50], whereas O^- oxidizes and eliminates C and Si species [51]. On the other hand, O_2 causes Si and C dangling bonds and oxycarbides linkages during dry thermal oxidation, which is inherently slower than wet (H_2O) oxidation [23]. It is observed that the oxidation rate of H_2O in wet thermal oxidation is higher than in dry (O_2) oxidation. It passivates Si and dangling bonds and removes carbon and oxycarbides bonds. However, too much accumulation of H^+ contributes to positive charge build-up at the SiO_2/SiC interface [23]. **Table 6**

shows reported ranges of electrical and reliability results for oxides grown in dry, wet and nitridation ambient on 4H-SiC. It confirms that when compared to other process conditions, wet nitrided has the lowest effective oxide charge density (Q_{eff}), the interface trapped charge (N_{it}), and a higher breakdown voltage. As a result, it is clear that wet nitridation conditions not only produce thicker gate oxides in a shorter duration but also produce greater gate oxide dependability in terms of lower traps and a higher breakdown voltage.

Table 5 The roles of C and Si species at the SiC interface during oxide growth in wet and dry oxidation ambient.

Reactions in gate oxides / Species	O^-	H^+	N^-
C passivation	X	√	√
C removal	√	X	√
Si passivation	X	√	√
Si removal	√	X	X
Si oxidation	√	X	X

Table 6 The reported ranges of electrical and reliability results for oxides grown in dry, wet and nitridation ambient on SiC.

Process ambient	$Q_{eff}(x10^{12})$	N_{it} $(x10^{12})$	Breakdown voltage (MV/cm) at 1 uA/cm
Dry	5 - 6 [52]	3 - 4 [53]	6 [26]
Wet	4 - 8 [54]	2 - 9 [55]	6 - 6.3 [21]
Dry Nitridation	1 - 5 [50,56,57]	1 - 4 [53]	6 - 6.5 [21,58]
Wet Nitridation	0.2 - 2 [21,59]	0.08 - 0.3 [21,59]	6 - 6.8 [20,21,59]

Conclusions

In this work, regression approaches, including linear and polynomial regression are used to generate models and formulations based on the extracted oxide thickness for a range of process temperatures and durations under various processing conditions; conventional (dry and wet oxidation), dry nitridation (N_2O and NO) and wet nitridation (HNO_3). The modelling and formulation were based on the extracted oxide thickness being above 50 nm for high-power applications. R^2 and MAPE techniques are used to assess the models' performance. When employing duration as the measurement parameter, polynomial regression, as opposed to linear regression, offers superior fitting accuracy. When using the polynomial method, the percentage of duration between the actual and calculated wet and dry thermal oxidation conditions is less than 10 %, as opposed to more than 10 % when using the linear regression method. The oxide thickness discrepancy between the calculated and actual thickness is less than 0.2 %.

The result of this work clearly demonstrates that gate oxide thickness can be extracted using linear and polynomial methodologies from silicon carbide-based wide-bandgap materials employing thermal oxidation durations at various temperatures for high power applications. The relationship between oxide thickness and process times and temperatures for dry and wet oxidation ambient shows that oxide growth occurs more rapidly in a wet environment. However, wet oxidation combined with nitrided elements makes a thicker gate oxide with higher reliability compared to other processing conditions. The roles of oxygen species as oxidizing agents, hydrogen, and nitrogen species as agents that passivate structural flaws at the bulk oxide and SiO_2/SiC interface are all included in the paper. The passivation effects of H^+ and N^- on the structural defects to the SiO_2/SiC interface are proposed as the likely cause of these improvements, which is the formation of stronger SiN and the removal of carbon and associated complex silicon oxycarbon bonds.

The models and formulations created as a result of this work can help researchers choose the necessary oxide thickness at different gate voltages, primarily for high-power applications. This study is projected to reduce processing time, costs, and material requirements in addition to eliminating the need for expensive experimental work to determine the oxide thickness on SiC during dry, wet, and nitrided thermal processing

conditions. As machine learning technology advances, the results of this work are suited to be integrated into semiconductor manufacturing tools.

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