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Comparative Study of Double Gate and Silicon on Insulator MOSFET by Varying Device Parameters

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Abstract

A comparative study of the single gate MOSFET (SG MOSFET), double-gate MOSFET (DG MOSFET) and silicon-on-insulator MOSFET (SOI MOSFET) is done using MOSFET simulation tool. Device simulation is done by varying different physical parameters of the device structure such as oxide thickness, channel length, temperature and different gate electrodes. Contour plots of SOI and DG MOSFET for electron concentration and potential at initial and final bias are simulated. The drain current vs gate voltage (I_d-V_g) characteristics performance simulations show that DG MOSFET is better than SOI MOSFET for different oxide thickness and channel length. It was further noticed that with an increase in the oxide thickness, drain current decreases for DG and SOI MOSFETs. When oxide thickness is reduced from 10 to 7 nm keeping all other parameters same, in DG MOSFET drain current increased by 49.49 % and in SOI MOSFET drain current increased by 66.6 %. When channel length is reduced from 80 to 75 nm in DG MOSFET drain current increased by 1.35 % and in SOI MOSFET drain current increased by 2 %. The performance simulations show that aluminium (Al) gate electrode is better than n^+ poly silicon (Si) and tungsten (W) for every MOSFET devices. With respect to aluminium gate electrode in DG MOSFET, for n^+ poly Si and tungsten, drain current decreased by 3.89 and 30.5 %, respectively and in SOI MOSFET, for n^+ poly Si and tungsten, drain current decreased by 3.84 and 34.61 %, respectively.

Keywords: MOSFET, SG MOSFET, DG MOSFET, Oxide layer, Simulation, SOI MOSFET

Introduction

Since more than 50 years, circuit miniaturization had been driven by Moore's law [1]. Circuit miniaturization aids to increase functionality, low cost, and portability. When doing miniaturization problems like short channel effect and high leakage current are faced which sets a limit for downscaling of the devices. However, the extension of scalability of devices has been achieved by expanding the present technologies, replacing previously used materials in transistors.

Different variants of MOSFET have been proposed. There are promising devices like ultra-thin body silicon-on-insulator (SOI), vertical transistor, FINFET, double-gate (DG) MOSFET and other nonclassical CMOS which have potential of downscaling the device parameters for the next few years. The application of these devices is for higher performance, higher transistor density and lower power density. Among all these variants of MOSFETs, this paper focuses primarily on DG and SOI MOSFET and further analyzed. DG MOSFET has better control as compared to SG MOSFET. For example, it has better control on the channel which reduces the short channel effect and leakage current. As compared to Single Gate (SG) MOSFET, SOI MOSFET [2] also have the advantages like reduced short channel effects, reduced leakage current, and better switching speeds due to a reduction in the drain-body capacitance. New transistor forms also seek to enhance the electrostatics of the MOSFET [3]. Device characterization, compact model and parameter extraction are the key challenges for design of DG and SOI MOSFET [4].

The technology roadmap for nanoelectronics, developed by the Information Society Technology Project of the European Commission, provides an excellent overview of nanoelectronics devices (future and emerging technologies) [5]. DGSOI is considered to have adequate features to make up nano-scale circuit design devices due to the short channel effects (SCEs) suppression, lower leakage current of the gate, higher drive current, and stronger sub-threshold values, among the many potential candidates for scaling [6,7]. In another investigation, comparison of SG MOSFET and DG MOSFET is done for parameters like drain current, quantum capacitance, mobile electrons [8]. The study on the comparison of multiple-gate SOI MOSFET using Monte Carlo simulation is done to reduce the short channel effect and leakage current is discussed in [9]. Furthermore, a study on surface potential, electric field, output conductance (g_m), total current density, and characteristic curves has been done. A comparison between undoped DG MOSFET, fully doped DG MOSFET, dual insulator DG MOSFET, graded channel DG MOSFET and gate stack DG MOSFET are done [10]. An analytical study was done on MOSFET scaling trends, challenges, and key associated metrology issues through the end of the roadmap are studied [11]. The efficiency of a double gate MOSFET (DG MOSFET) based on novel channel materials was researched in a study by Prasher *et al.* [12]. In recent work a study on electrical characteristics of DG MOSFET is done for varying various device parameters like oxide thickness, doping concentration and gate-dielectrics [13]. This paper analyzed trade-offs involved in the selection of parameters for optimum characteristics of the DG MOSFET. Performance analysis of graded channel DG MOSFET is done to investigate impact of channel engineering on double gate MOSFET [14]. A comparison of DG MOSFET and SOI MOSFET is done. Various parameters like the electric field, charge carrier density, drive current, drain current are compared by varying channel length, oxide thickness, gate electrode type for different types of MOSFET devices to get the best performing device under various conditions.

MOSFET architecture and simulation framework

Double gate (DG) MOSFET

A double-gate MOSFET (DG MOSFET) is the same as a typical metal oxide semiconductor but with 2 gates. **Figure 1** displays the schematic of DG MOSFET. The key challenge of short channel effect in nanoscale single gate devices can be solved by multi-gate architectures such as double gate, tri-gate and gate all around the structure [15]. The DG MOSFET configuration minimizes short-channel effects, allowing devices up to 10 nm gate length to be downscaled more aggressively [16]. The current is regulated by both the gates in the DG MOSFET, as shown in **Figure 1**. One is known as the top gate on the upper side and the other is known as a bottom gate on the lower side of the channel. It gives better control of the channel by the gate electrodes [17]. This means that no part of the channel is far away from a gate electrode. Because of 2 gates, DG MOSFETs are more resistant to short channel effects (SCEs) and have high conductivity, which provides better channel control compared to SG MOSFET. And due to this property, it is possible to downscale the dimensions double-gate MOSFET for the same channel thickness. when compared to SG MOSFETs [18].

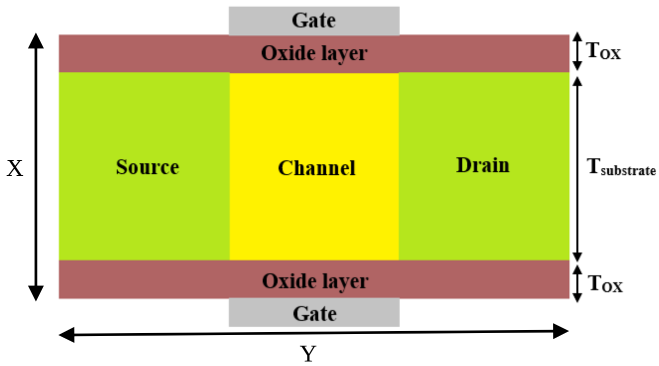


Figure 1 Schematic of DG MOSFET.

Silicon on insulator (SOI) MOSFET

The schematic diagram of the SOI MOSFET is shown in **Figure 2**. In SOI technology, it doesn't change the fundamental geometry of the transistor. In SOI, the creativity lies in the addition of a thin layer of insulator which is known as a buried oxide layer that lies below the channel which is the main difference between conventional MOS structure and SOI MOS structure that isolates the body from the substrate and hence leakage current is reduced. Reduction in the channel length of SOI MOSFET is possible as compared to conventional MOSFET, as it reduces the effect of SCE and leakage current [19]. Working of SOI MOS is very much similar to bulk MOSFET.

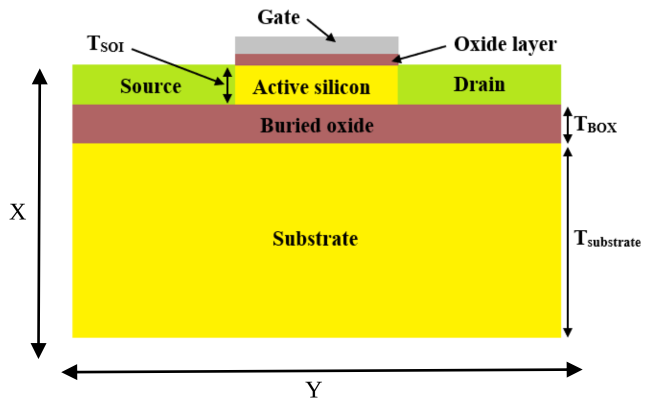


Figure 2 Schematic of SOI MOSFET.

By nature of the structure, SOI gives better transistor electrostatic characteristics than conventional bulk technology. SOI technology enables control of the behavior of transistors by polarizing the substrate under the device, similar to the body bias of the bulk MOSFET. In bulk technology, body biasing is very limited, due to parasitic current leakage and inefficiency at reduced transistor geometry. With the benefits of the construction design of SOI and its ultra-thin insulator layer, biasing is much more efficient. Due to the presence of buried oxide layer, in body biasing the substrate below the buried oxide layer acts as another gate leading to a double gate type of structure, resulting in faster transmission of electrons from source to drain.

Method of simulation

MOSFET tool simulates the current-voltage characteristics for DG and SOI MOSFET for a variety of different device sizes, geometries, doping concentration and temperature. DG MOSFET and SOI MOSFET devices are simulated by varying their physical parameters using the MOSFET tool on nanhub.org [20]. To analyze the limit of downscaling of physical dimensions of DG and SOI MOSFET, the simulation was achieved through the tool. The MOSFET tool simulates the drain current-gate voltage (I_d-V_g) characteristics and contour plot for DG and SOI MOSFET and their results analyzed.

Table 1 Input parameters used for DG and SOI MOSFET.

Input parameters	Simulation values
Source/Drain length	50 nm
Channel length	75, 80 nm
Oxide thickness	7, 10 nm
Junction depth	20 nm
Substrate thickness (For SOI MOSFET)	50 nm
Buried oxide thickness (For SOI MOSFET)	50 nm
Source doping concentration	$2\times e^{+20}$ /cm^3
Drain doping concentration	$2\times e^{+20}$ /cm^3
Substrate doping concentration	$5\times e^{+16}$ /cm^3
Channel doping concentration	$1\times e^{+18}$ /cm^3
Device width	1000 nm
Ambient temperature	200, 400 K
Transport model	Drift diffusion
Gate electrode	n^+ poly Si, Tungsten, Al

Results and discussion

The observations and analysis were made as a result of the simulation of DG and SOI MOSFET devices. Performance simulation of I_d-V_g characteristics is analyzed by varying oxide thickness, channel length, temperature and gate electrodes among DG or SOI MOSFET. An observation is made which one gives better characteristics under the given parameters. And what variation occurs in the device between initial and final bias can be observed in the contour plots.

I_d-V_g characteristics

Among the SG, DG and SOI MOSFET, DG MOSFET has better performance as compared to SG and SOI MOSFET as shown in **Figure 3**. The simulation results are shown below for DG MOSFET and SOI MOSFET devices for the performance analysis of drain current. The results are simulated at different gate voltage, at a constant drain voltage of 1 V with varying different parameters of channel length, oxide thickness, ambient temperature and the gate electrode.

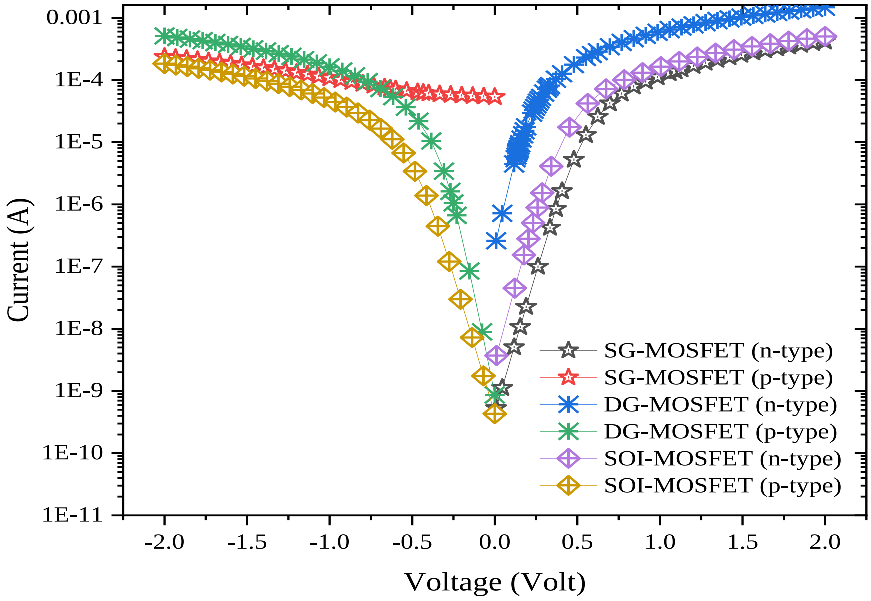
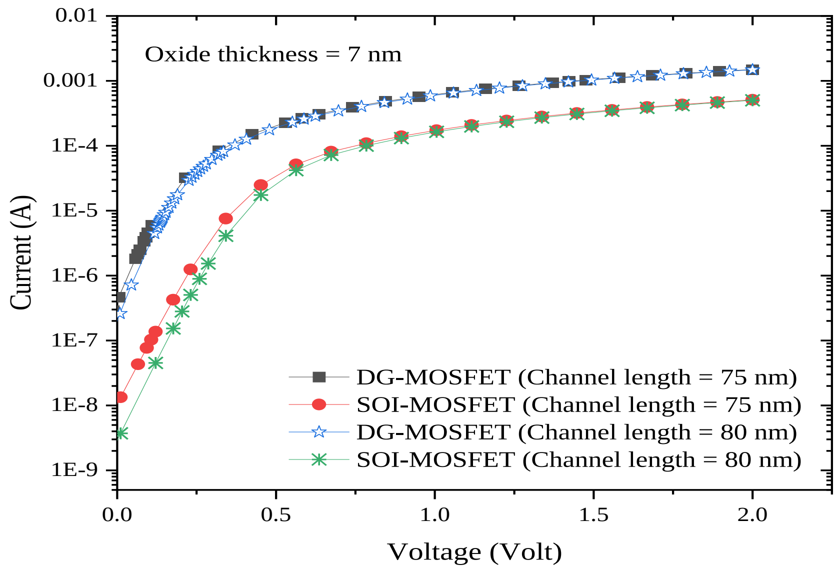


Figure 3 Drain current vs gate voltage (I_d-V_g) characteristics.

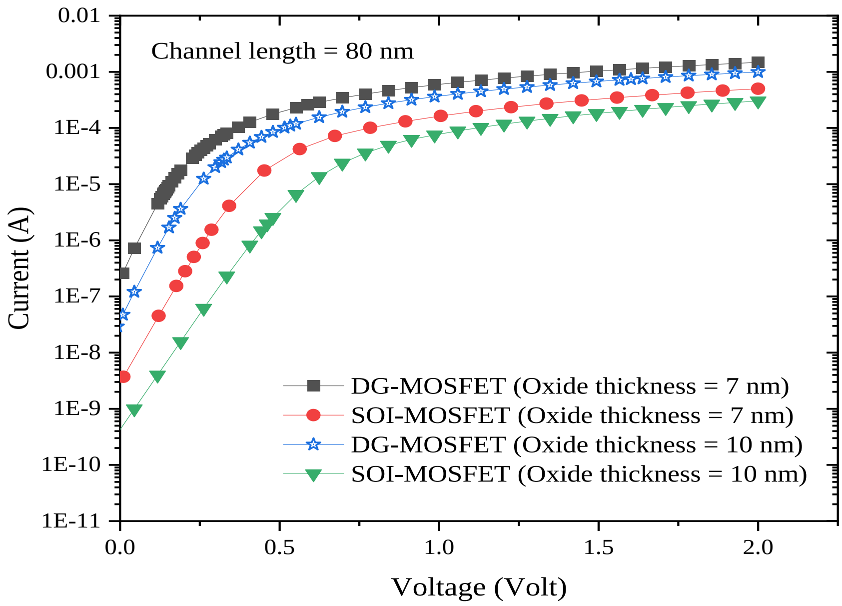
DG MOSFET and SOI MOSFET show a half parabolic-like curve for I_d-V_g characteristic in **Figure 4(a)**. With the reduction in oxide thickness, it is observed from the simulation and the graph plotted that the drain current of both MOSFET devices increases. It can also be observed that the DG MOSFET has more drain current when compared to SOI MOSFET. The drain current for DG MOSFET at 2V and the constant drain voltage of 1V for oxide thickness of 7 nm and a channel length of 80 nm is 1.48 mA and for SOI MOSFET the drain current is 0.5 mA. Hence DG MOSFET has more drain current than SOI MOSFET. The drain current for DG MOSFET at 2V for channel length of 80 nm and oxide thickness of 10 nm is 0.99 mA and for SOI MOSFET is 0.30 mA. It shows that DG performs better than SOI while comparing it with the same oxide thickness.

In **Figure 4(b)**, simulation of both devices for a channel length of 80 and 75 nm at a constant drain voltage of 1V with oxide thickness of 7 nm is shown. The drain current for DG MOSFET at 2V for channel length of 80 nm and oxide thickness of 7 nm is 67.74 % more than that of SOI MOSFET and for channel length 75 nm, drain current for DG MOSFET is 85.83 % more than that of SOI MOSFET. It can be seen that the drain current is more in DG MOSFET as compared to SOI MOSFET. From this, it can be demonstrated that when oxide thickness increases than the drain current decrease as charge decreases on surface due to less capacitance. Similar result can be compared with the recent work on electrical characteristics of Double-Gate MOSFET, in which drain current of 0.014 mA is observed for oxide thickness of 4 nm and V_d = 2V. Also, same trend of increasing drain current can be seen when oxide thickness is decreased [13]. In another study on DG MOSFET, similar outcome of 0.58 mA can be observed for oxide thickness of 0.8 nm and V_g = 0.8V [14]. Likewise, in study of DG MOSFET at 20 nm channel length 0.602 mA is obtained at V_d = 0.1V and oxide thickness of 1 nm and V_g = 1V [17].

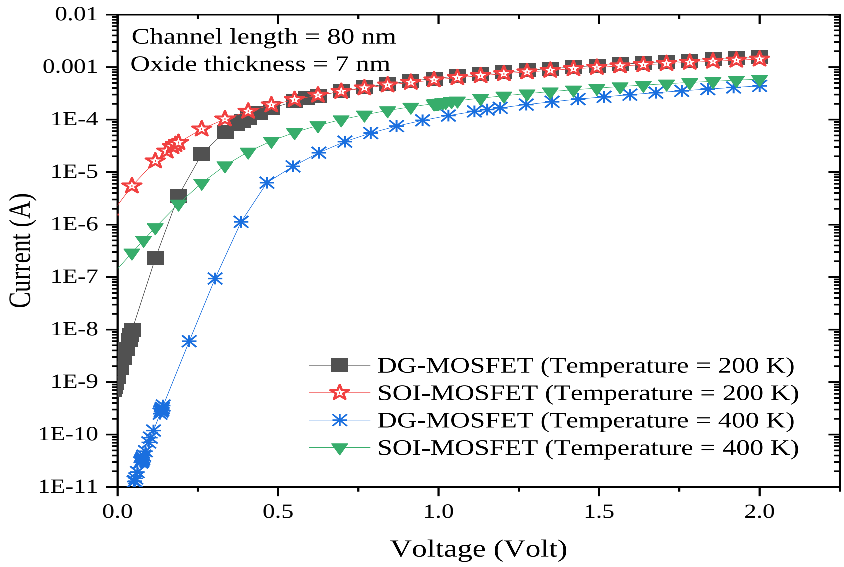
The MOSFET devices are affected due to temperature variations that cause changes in the drain current of the device. In **Figure 4(c)**, analysis is done for the DG and SOI MOSFET based on ambient temperature parameters. For high values of Gate Voltage, the drain current decreases with temperature rise, i.e., the MOSFET exhibits a negative coefficient of temperature at greater values of gate voltage. At the lower gate to source voltages, the current increases with temperature. So, the ON current decreases with temperature and the leakage current or OFF current increases with temperature. Hence the I_d-V_g characteristics are worst at high temperatures [21]. The variation of DG and SOI MOSFET I_d-V_g characteristic with different temperatures is shown in **Figure 4(c)**.



(a)



(b)



(c)

Figure 4 Drain current vs gate voltage (I_d-V_g) characteristics (a) Oxide thickness 7 nm and varying channel length, (b) Channel length 80 nm and varying oxide thickness, and (c) Channel length 80 nm, oxide thickness 7 nm and varying temperature.

Varying the threshold voltage (V_{th}) of the transistors is ideal for optimizing circuit efficiency. And for controlling the V_{th} of MOSFET, the work function (WF) of the metal-gate electrode is modified. The source/drain formed by ion implantation and gate electrode reflects the regions in which voltages are applied to a MOSFET. As per the required work function of the gate, specific materials like silicide material or metal composites are used. The basic materials used to rely on the required work function of the gate. The combined simulation result of DG and SOI MOSFET is shown in **Figure 5** for the different gate electrodes. From the analysis, it can be seen in the graph that DG MOSFET and SOI MOSFET gives the best I_d-V_g characteristics for the aluminium gate electrode. Thus, the aluminium gate electrode should be beneficial to get a better drain current as compared to the gate electrode of n^+ poly silicon and tungsten.

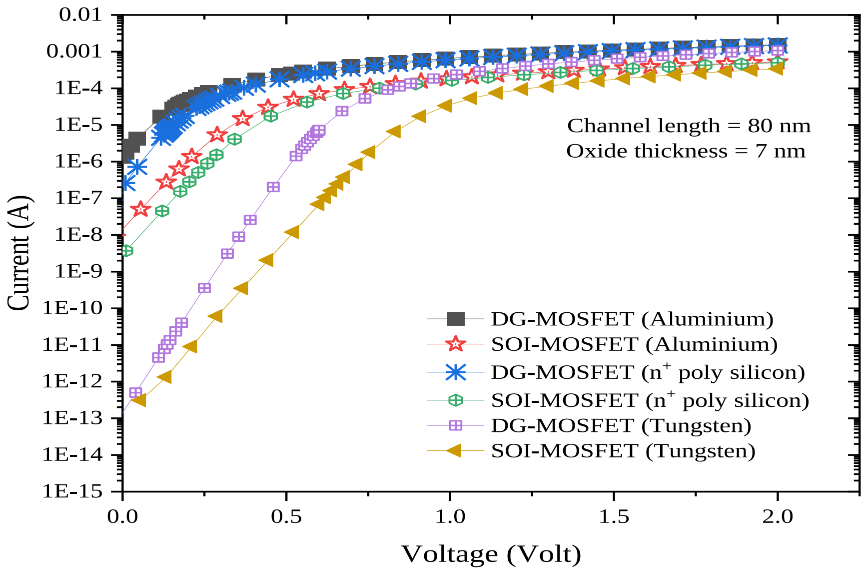
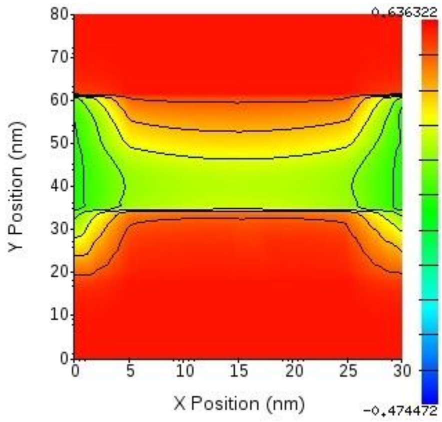


Figure 5 Drain current vs gate voltage (I_d-V_g) characteristics.

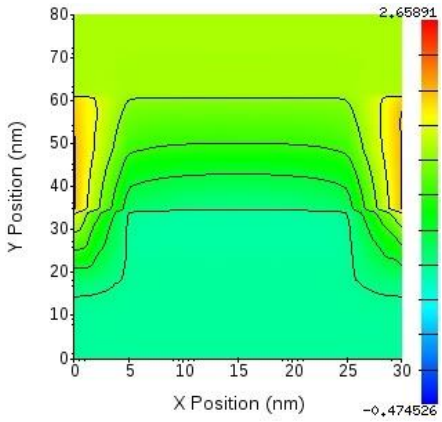
Observation of contour plot for potential and electron concentration

A contour plot is a graphical method for representing a 3D surface called contours. It is plotting of constant z slices in a 2D format. Contour plots for DG and SOI MOSFET have been obtained and their respective plot is shown in colormap range in log10 scale. Here, Y-axis shows along the length of the device while X-axis represents the height of the device in each contour plot (**Figures 1** and **2**).

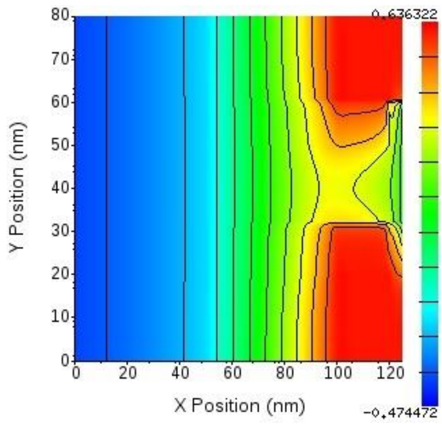
Figures 6(a) and **6(b)** shows the contour plot of potential for n-type DG MOSFET for initial as well as final bias. From the figure, the change in potential between drain and source can be observed. At initial bias, when drain voltage $V_d = 0$ V, the source and drain are at the same potential. While comparing at the final bias, when drain voltage $V_d = 1$ V, the drain is at higher potential as compared to the source. Similarly, for n-type SOI MOSFET, at initial bias, the source and drain are at the same potential whereas at final bias drain is at much higher potential compared to the source shown in **Figures 6(c)** and **6(d)**.



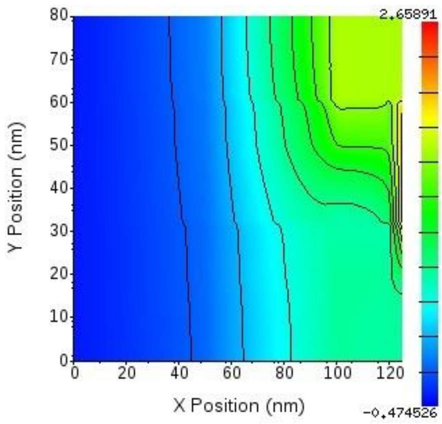
(a)



(b)

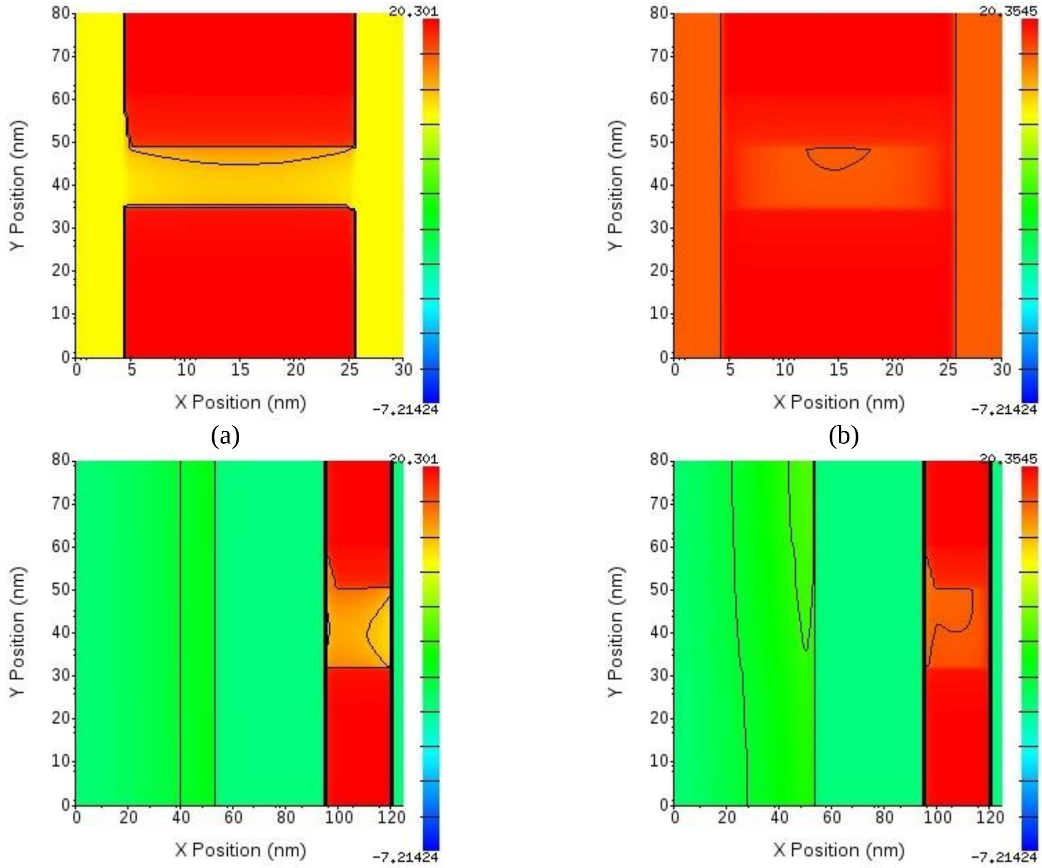


(c)



(d)

Figure 6 Contour plot of potential of n-type MOSFETs: (a) DG MOSFET at Initial Bias (Vd = 0 V), (b) DG MOSFET at Final Bias (Vd = 1 V), (c) SOI MOSFET at Initial Bias (Vd = 0 V), and (d) SOI MOSFET at Final Bias (Vd = 1 V).



(c) (d)

Figure 7 Contour plot of electron concentration of n-type MOSFETs: (a) DG MOSFET at Initial Bias (Vd = 0 V), (b) DG MOSFET at Final Bias (Vd = 1 V), (c) SOI MOSFET at Initial Bias (Vd = 0 V), and (d) SOI MOSFET at Final Bias (Vd = 1 V).

Figure 7 shows the contour plot of electron concentration for n-type DG MOSFET and n-type SOI MOSFET. In **Figures 7(a)** and **7(b)**, the channel which is at the position from 35 to 50 nm along the Y-axis and from 5 to 25 nm along the X-axis at initial bias has a lower concentration of electron than that of the final bias. That is because of applying a voltage at the drain, the electrons that are accumulated in the channel region due to gate voltage gets drained at the drain side, which results in a rise in concentration in that region. The same can be observed for n-type SOI MOSFET in **Figures 7(c)** and **7(d)**.

Conclusions

In this work, we have studied, simulated and investigated various MOSFET devices (SG, SOI and DG) by optimizing various parameters such as oxide thickness, channel length, temperature and gate electrodes. Performance analysis of SOI MOSFET and DG MOSFET is done by varying different parameters such as oxide thickness, channel length, temperature and gate electrodes. Contour plots for SOI and DG MOSFET devices for electron concentration and potential at initial and final bias are simulated. In the contour plot, we can observe the variation of colour range that occurred in the device between initial and final bias. The performance simulations of drain current show that DG MOSFET is better than SOI MOSFET for different oxide thickness (7 and 10 nm), channel length (75 and 80 nm). When oxide thickness is reduced from 10 to 7 nm, in DG MOSFET drain current increased by 49.49 % and in SOI MOSFET drain current increased by 66.6 %. When channel length is reduced from 80 to 75 nm in DG MOSFET drain current increased by 1.35 % and in SOI MOSFET drain current increased by 2 %. With respect to aluminium gate electrode in DG MOSFET, for n^+ poly Si and tungsten, drain current decreased by 3.89 and 30.5 %, respectively and in SOI MOSFET, for n^+ poly Si and tungsten, drain current decreased by 3.84 and 34.61 %, respectively.

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