

## Modeling of 7 Nano Meter Fin Field Effect Transistor for Evaluation of Fringe & Oxide Capacitance

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### Abstract

Fin-FET are insusceptible to short channel effects punch through, threshold voltage, leakage current but their concerts at high frequencies are conceded due to durable fringing field between gate and source with drain area. Because of high-technology progression, the gate construction of MOSFET has been upgraded from planar to nonplanar with an enrichment in the number of monitoring gates multiple gates on 3 sides. In this paper we mention Fin-FET assembly for high frequency applications.

MOS-FET plays very energetic role but scaling of device affected on performance parameters like speed and power. Fin-FET is non planar novel device to solve the short channel effects which occurs due to scaling. Non-planar structure of Fin-FET parasitic capacitances like gate oxide overlap and fringe capacitance makes adverse effect like lower switching speed of device, making result on delay ion and ioff of device. In this paper we planned Fin-FET design procedure to measure oxide and fringe capacitance with low k dielectric spacer thickness and increase ion to recover device driving ability. Effect on threshold voltage having observed with low k spacer at least count of 0.051 V. By using 4.65 eV metal gate work function with front, top and back gate we control leakage current and threshold voltage. Seven nano meter gate length Fin-FET is design We measured oxide capacitance of 0.464 F for 19.28 GHz and fringe capacitance (69.66 nf) for 4.88 GHz frequency by designing the Fin-FET with high-K SOI MOSFETs which support 11.4 nA leakage current to improve the speed of the processor.

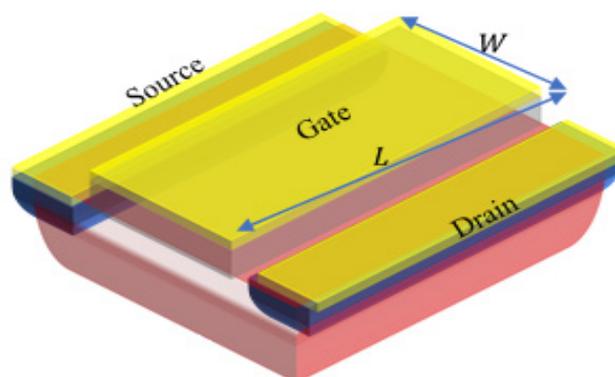
In this research work, design topologies of Single Finger Fin Filed Effect Transistors are discussed and evaluate the probable result of fringe and parasitic capacitance from fringing area on the device. By using geometry of device like fin width, height, thickness and multiple fingers we measure the fringe capacitance and oxide capacitance of designed Fin-FET.

**Keywords:** CMOS technology, Fin-FET, Parasitic, Thickness, Geometry, Dielectric

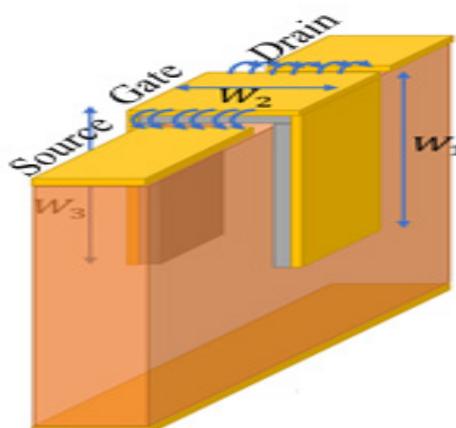
### Introduction

As per the Moore's law, the degree of transistors in CMOS application are double for each 18 months, in study the scaling of the devices has been done to site a high number of transistors on the chip. Flat transistors structure has unwanted effects like mobility degradation, gate tunneling, giant leakage currents. From former data, as transistor size shrink up to 22 to 10 nm. Double-gate MOSFET is outstanding device for controlling focus of VLSI study since, it can be scaled to the direct channel dimension likely for a specified gate width. Due to double gate structure of MOSFET, the problem of misalignment of top or bottom and front or posterior gate occurs. Fin-FET is one of the innovative approaches having better performance characteristics such as Low leakage current, upgraded short-channel effect.

Multiple fingers are used in Fin-FET, fingers of Fin-FET needed to be stripper due to which sprinkling of dopants increases. We design the triple gate rectangular Fin-FET (TG-Fin-FET). Due to small thickness of fins, the drain current is concentrated as the movement of charge carriers by reducing on current, so to growth the drain current, the quantity of fins has to be improved. **Figure 1** shows the planar horizontally aligned MOSFET structure which contain gate drain and source. **Figure 2** shows Non planar vertically aligned Fin-FET model which contains 3 gates on front, back and top side with drain and source terminal.



**Figure 1** MOSFET construction.



**Figure 2** Fin-FET construction.

### Device construction

FET can be used at high frequencies and provides carrier propagation through the channel. At small gate sizes, this is possible due to collision free-transport of carriers through the channel known as Ballistic Transport. Sinking the gate length has other undesired things which have to be minimized. One of the most important effect of Gate Length scale down is decrease in Gate Coupling Factor. Gate Coupling Coefficient or Kappa is the portion of control of vertical field on carriers.

$$Kappa = \frac{C_{oxWL}}{C_{oxWL} + C_{depletion}} \quad (1)$$

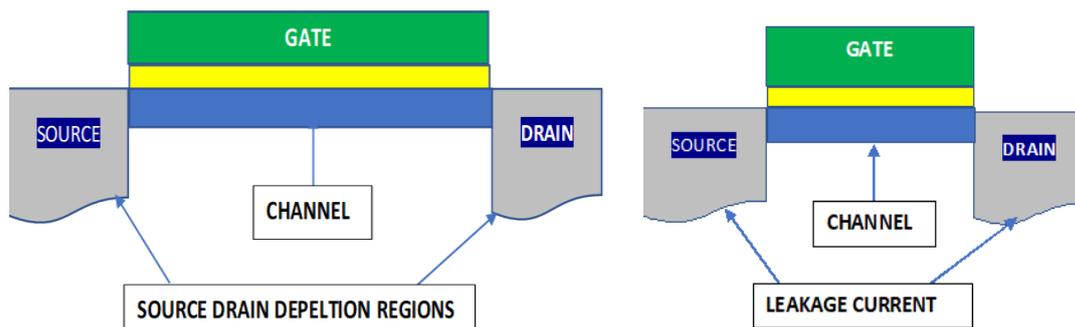
$C_{oxWL}$  is gate oxide capacitance

$C_{depletion}$  is the depletion capacitance of the depletion region under the channel.

$C_{depletion}$  is designed to be 5 - 10 % of the  $C_{oxWL}$ .

Typically, Kappa is in the range of 0.85 to 0.95.

As the gate length scales in nano meter regime, gate oxide capacitance leaks and gate coupling coefficient drops. As the Fin-FET having perpendicular arrangement, field drops control over the carriers and device cannot be switched off. To protect the loss of the control over the gate in design we use high dielectric constant oxide for the gate which gives better result for reducing leakage current. Hafnium oxide with the dielectric constant of 25 is preferred and silicon dioxide ( $\epsilon_r = 3.7$ ) and silicon nitride ( $\epsilon_r = 8.5$ ). Gate oxide thicknesses of the command of a nano-meter is used in typical devices. Another modification is that the device has non-planar in assembly but channel is from stretched up like a fin. The Gate is placed around the channel on 3 sides (from top, back and front). This is referred to as Fin-FET. DIBL effects can be lowered by heavy doping of the channel and growing metal semiconductor work function. Metal semiconductor work function directly affects the threshold voltage. **Figure 3** shows long channel and short channel device which represents how source and drain are closer to each other.



**Figure 3** Long channel device and short channel device.

Long channel devices have large gate lengths. The output characteristics has 3 distinct regions;

- 1) Triode region
- 2) Saturation region
- 3) Breakdown region

In triode region,

$$I_d = \frac{\mu_n C_{ox} W}{2 L} [2V_{ov} V_{ds} - V_{ds}^2] \tag{2}$$

where  $I_d$  is drain current

$C_{ox}$  is oxide capacitance

$W$  is fin width

$L$  is gate length

$V_{ov}$  is overdrive voltage,

$V_{ds}$  is drain to source voltage,

$\mu_n$  is mobility.

$$V_{ov} = (V_{gs} - V_t) \tag{3}$$

where,  $V_{gs}$  is gate to source voltage,

$V_t$  is threshold voltage.

Pinch-off occurs at  $V_{ds} = V_{ov}$ , At pinch-off, drain current is given by;

$$I_{ds} = \frac{\mu_n C_{ox} W}{2 L} V_{ov}^2 \tag{4}$$

In saturation region,

$$I_d = I_{ds} (1 + \lambda (V_{ds} - V_{ov})) \tag{5}$$

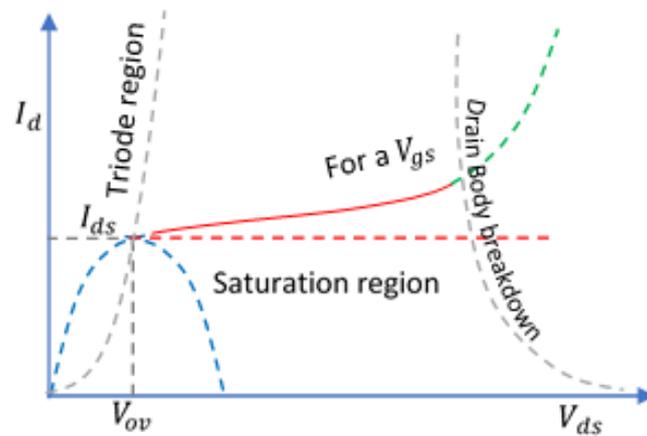
$$\lambda = \frac{K_{ds}}{2L\sqrt{V_{ds} - V_{ov} + \phi_0}} \tag{6}$$

In breakdown region, the drain to body reverse biased junction breaks down leading to leakage of drain current to the body.

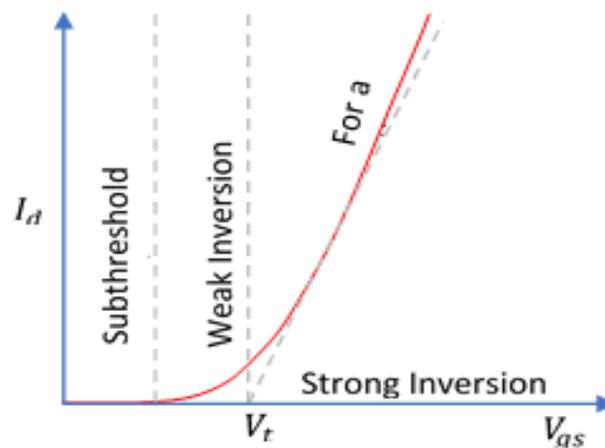
There are 3 distinct regions of transfer characteristics;

- 1) Subthreshold region of operation
- 2) Weak inversion
- 3) Strong inversion

There is no clear boundary between these regions. Operating or beginning voltage of the scale device is not uniquely defined.



**Figure 4** Output characteristics of MOSFET.



**Figure 5** Transfer characteristics of MOSFET.

#### Short channel effects

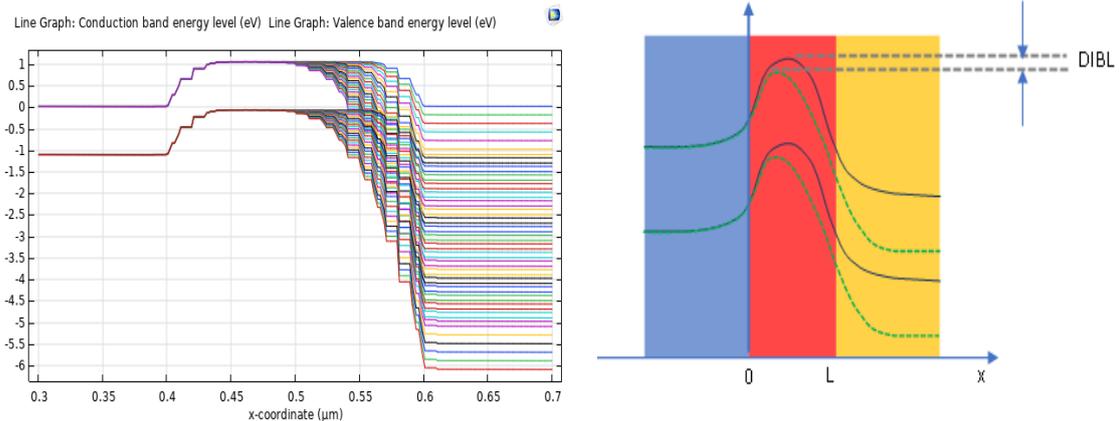
In long channel transistor when we vary voltage from lowest to highest range, observes increase in drain voltage which leads in drain current in off state and same increase in on state current. So we observe in long channel device same increase in on state and off state and Sub threshold slope. Several shorts channel effects are;

- 1) Drain induced barrier lowering
- 2) Punch through
- 3) Mobility degradation

Sub-threshold leakage current

#### Drain induced barrier lowering

In extended drain gate length devices, threshold voltage is permitted to close the drain to source voltage. In rapid channel devices, the drain to source voltage sinks the threshold voltage. This is referred to drain induced barrier lowering. The simulated results of DIBL shown in **Figure 6** by measuring 74.49 mv from design of Fin-FET.



**Figure 6** Drain induced barrier lowering graph.

### ***Punch through***

Light doping of channel can cause the depletion region at drain body junction to completely span the channel beginning carriers to punch through under the control of drain to source voltage with least or no control of the gate to source voltage. This is referred to as punch through.

### ***Mobility degradation***

For overdrive voltages higher than the drain to source voltage, the drain current does not follow the square law nature. This is mainly due to carrier-to-carrier interaction when vertical fields due to gate to source voltage are stronger than the horizontal fields. The effect is visible in output characteristics as drain current in triode region being flatter than the parabolic nature. In transfer characteristics it is more pronounced for gate to source voltage higher than the drain to source voltage plus threshold voltage.

$$\mu_n = \frac{\mu_{n0}}{1 + \eta \frac{V_{ov}}{V_{DS_{sat}}}} \quad (8)$$

$\mu_n$  is mobility of electrons

$V_{ov}$  is overdrive voltage

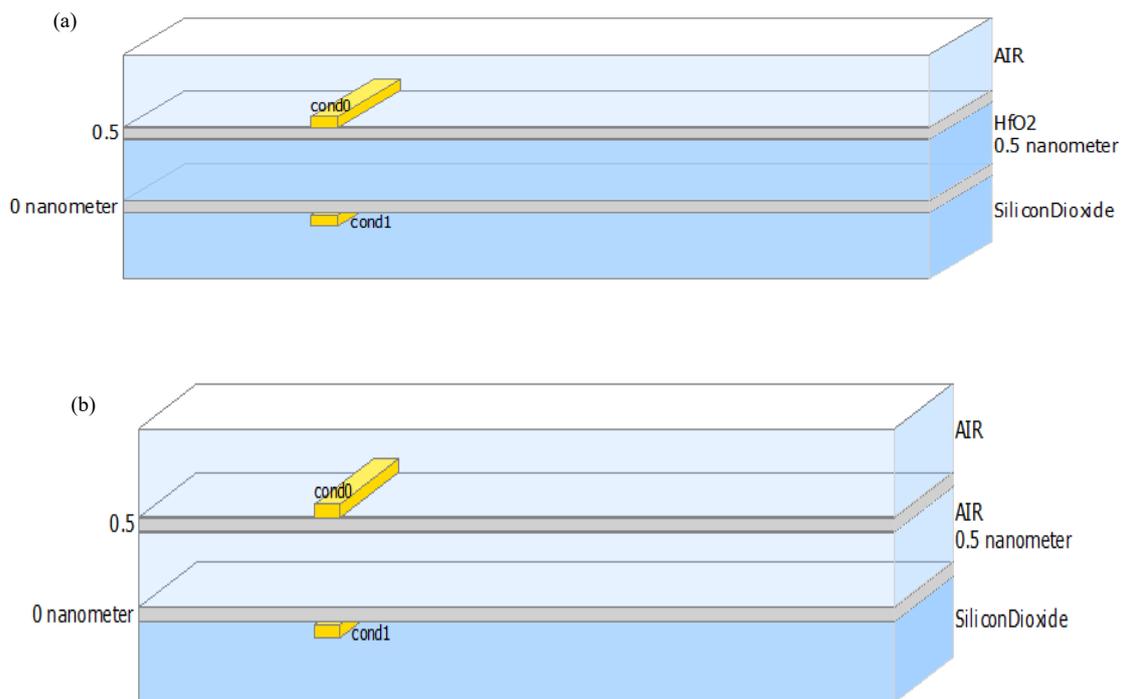
$V_{DS_{sat}}$  is drain to source saturation voltage

### ***Sub-threshold leakage current***

For gate to source voltage lower than the operating voltage, the device is supposed to be switched off. But this is not so because there are carrier paths between source and drain, are not below the switching of the gate to source voltage. Besides leakage currents, in absence of a channel, the structure is a parasitic bipolar with small forward current gain. This current is an exponential function of Gate to Source Voltage. From device design of 5 nm fin thickness and 7 nm gate length we found 14.69 nA leakage current which improves the performance of the device.

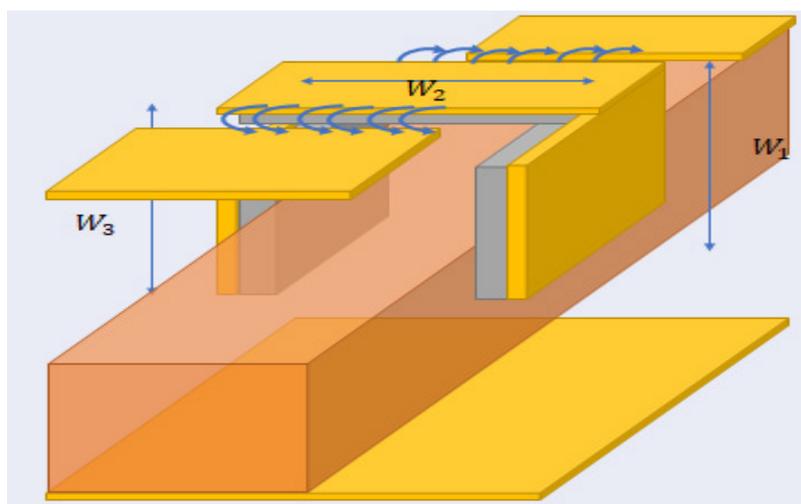
### ***Device design***

The Fin-FET device model are used for the simulation, the structure shown in **Figure 7**. The corresponding plane structure of device (i.e., through the identical channel length  $L_g = 7$  nm, effective oxide thickness = 1.2 nm) has been located such that the strategies have the identical  $V_t$  (~ to 0.2 to 0.3 V) as that of Fin-FETs. Then the main thought of this work is organized the epi associated with fringe capacitance. The fin promotion of the Fin-FET device is 60 nm. In this part, we develop the gate electrode depth and the gate underlap to weaken the fringe capacitance. We study the scale device to 7 nm and provided the size of fringing capacitance. In our investigation, we formulate  $\text{SiO}_2$  as the dielectric material. All device and circuit simulations were performed using a ADS-2020 device simulator. We used 7-nm (gate length) device for all our study.

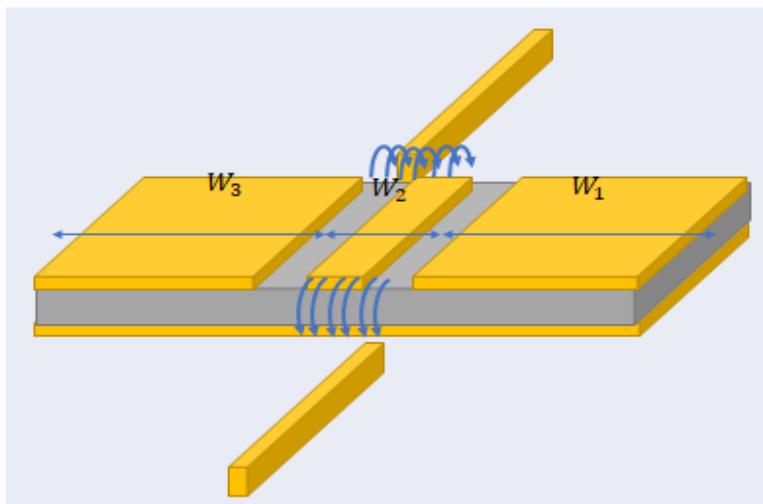


**Figure 7** (a) Structure of Fin-FET for capacitance measurement. (b) Geometry structure of Fin-FET for capacitance measurement.

Operative parasitic and fringe capacitance was computed by conformal mapping method. Designs are stabilized to the standards equivalent to the gate thickness  $T = L = 7$  nm. Physical Model use for calculation of fringe and oxide capacitance shown in **Figure 8** and extraction simplification with  $W_1$ ,  $W_2$  and  $W_3$  represent in **Figure 9**.



**Figure 8** Physical model for valuation of fringing capacitance.



**Figure 9** Extraction simplification for valuation of fringing capacitance.

Total gate oxide capacitance does not enter in drain current computations but for gate source capacitance;

$$C_{gs} = 2/3 WLCox \tag{9}$$

where,

$$W = (W1 + W2 + W3) \times nf \tag{10}$$

Gate to drain capacitance is given by;

$$C_{gd} = t_{fin} C_{fp} nf \tag{11}$$

where,  $t_{fin}$  is thickness of fin,  $nf$  is number of fingers. It can be seen that the fringe capacitance decreases logarithmically with gate width.

**Result and discussion**

From the geometry design of Fin-FET, we measure the value of fringe capacitance and oxide capacitance and simulate the S parameters with high frequency mode in GHz. From the result of simulation, we found very small value of ( $C_{ox}$ ) oxide capacitance 0.454 F at very high frequency of 19.28 GHz whereas at low frequency of 4.88 GHz found 56 PF of fringe capacitance, as number of fins increases the value of fringe capacitances are reduces. From the design of Fin-FET we calculate the oxide capacitance which is 0.464 F for 19.28 GHz frequency which is observe in **Figures 10 and 12**.

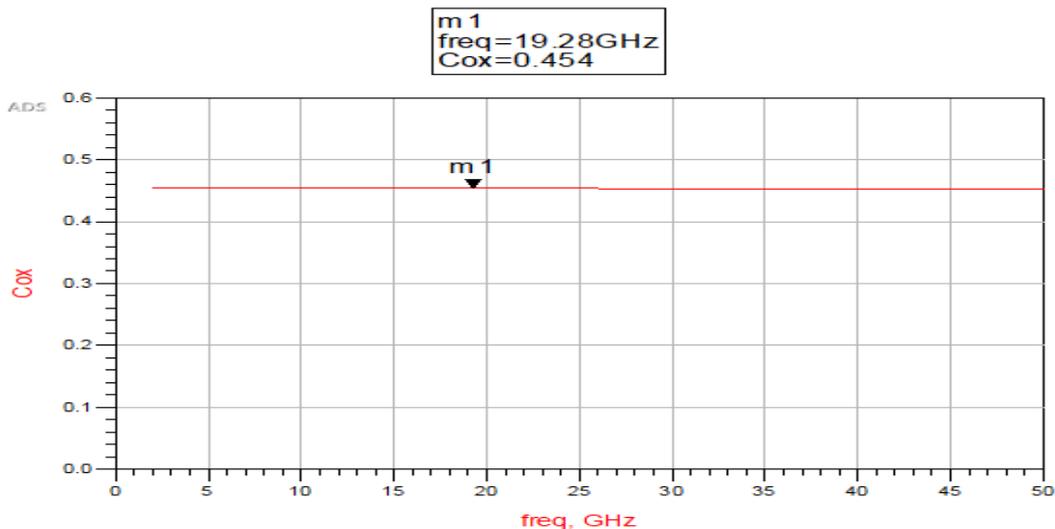


Figure 10 Oxide capacitance measurement.

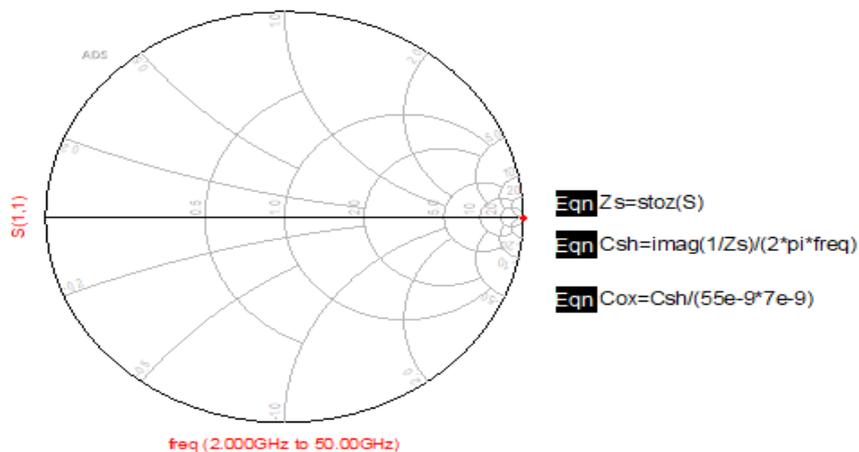


Figure 11 Fringe capacitance measurement.

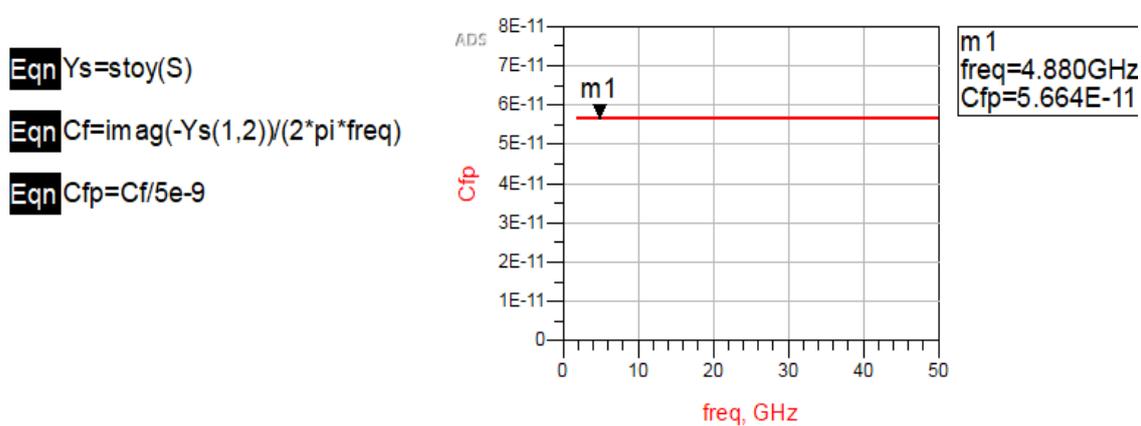


Figure 12 Oxide capacitance measurement.

## Conclusions

We have measured the values of oxide 0.464 F for 19.28 GHz and fringe capacitance (69.66 nf) for 4.88 GHz frequency by designing the Fin-FET with fully depleted high-K SOI MOSFETs. By developing an internal fringe capacitance and result terms for outside potential and threshold voltage with the effect of the internal fringe capacitance. This may find the device arrivals and performance and identify this result exactly for high-K gate dielectric SOI MOSFETs. Our model can be easily implemented in a ADS to include this conclusion.

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## References

- [1] TC Carusone, DA Johns and KW Martin. *Analog integrated circuit design*. 2<sup>nd</sup> ed. John Wiley & Sons, New Jersey, 2012, p. 816.
- [2] JM Rabaey, A Chandrakasan and B Nikolic. *Digital integrated circuits, a design perspective*. 2<sup>nd</sup> ed. Pearson Education India, Delhi, India, 2016.
- [3] Y Sun, Z Liu, X Li, J Ren, F Zheng and Y Shi. Analytical gate fringe capacitance model for nanoscale MOSFET with layout dependent effect and process variations. *J. Phys. D Appl. Phys.* 2018; **51**, 275104.
- [4] S Salas and JC Tinoco. Fringing gate capacitance model for triple-gate Fin-FET. *In: Proceedings of the 2013 IEEE 13<sup>th</sup> Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Austin, Texas. 2013, p. 90-2.
- [5] CR Manoj, AB Sachid, F Yuan, CY Chang and VR Rao. Impact of fringe capacitance on the performance of nanoscale Fin-FETs. *IEEE Electron Dev. Lett.* 2010; **31**, 83-5.
- [6] D Bhattacharya and NK Jha. Fin-FETs: From devices to architectures. *Adv. Electron.* 2014; **2014**, 365689.
- [7] AN Bhoj, RV Joshi and NK Jha. 3-D-TCAD-based parasitic capacitance extraction for emerging multigate devices and circuits. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* 2013; **21**, 2094-105.
- [8] T Yoon, KK Choe, KW Kwon and SY Kim. Performance optimization study of Fin-FET's considering parasitic capacitance and resistance. *J. Semicond. Tech. Sci.* 2013; **14**, 525-36.
- [9] T Yoon, SY Joo, KW Kwon and SY Kim. Modeling of parasitic fringing capacitance in multi-finger Fin-FETs. *IEEE Trans. Electron Dev.* 2013; **60**, 1786-9.
- [10] SS Rodriguez, JC Tinoco, AG Martinez-Lopez, J Alvarado and JP Raskin. Parasitic gate capacitance model for triple-gate Fin-FETs. *IEEE Trans. Electron Devices.* 2013; **60**, 3710-7.
- [11] A Korobkov, S Member, A Agarwal and S Venkateswaran. Efficient Fin-FET device model implementation for SPICE simulation. *IEEE Trans. Comput. Aided Des. Integrated Circ. Syst.* 2014; **33**, 1696-9.
- [12] SY Jang, SK Kwon, JK Shin and JN Yu. Decrease of parasitic capacitance for improvement of RF performance of multi-finger MOSFETs in 90-nm CMOS technology. *J. Semicond. Tech. Sci.* 2015; **15**, 312-7.
- [13] P Jay and AD Darji. Analysis of the source drain parasitic resistance and capacitance depending on geometry of FinFET. *In: Proceedings of the 11<sup>th</sup> Conference on Ph.D. Research in Microelectronics and Electronics*, Glasgow, Scotland. 2015, p. 298-301.
- [14] A Nakamura, N Yoshikawa, T Miyazako and T Oishi. Layout optimization of RF CMOS in the 90 nm generation by a physics-based model including the multi-finger wiring effect. *In: Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium*, San Francisco, California. 2006, p. 419-22.
- [15] I Kwon, M Je, K Lee and H Shin. A simple and analytical parameter extraction method of a microwave MOSFET. *IEEE Trans. Microw. Theor. Tech.* 2002; **50**, 1503-9.